

ZRMAE/ZEMAE

Juno/Iakros 10AN/10ANG

LA-A551P REV 1.0 Schematic

AMD KABINI Quad Core 25W for UMA+DIS
AMD KABINI Quad Core 15W
2013-07-05 Rev 1.0

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AMD GPU

AMD Sun Pro M2, 64bit with 1GB DDR3(2Gbit)
AMD Sun Pro M2, 64bit with 2GB DDR3(4Gbit)

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PCIe Gen2 X4
5Gbps

LVDS/eDP Conn

page 20

DP0 X4

HDMI Conn
(1.4b & 3D)

page 21

DP1 X4

PCIeMini Card For WLAN

PCIe port 2
page 23

PCIe Gen1 X1
APU SMBUS
2.5bps

RTL8106E 10/100M

PCIe port 1
page 25

PCIe Gen1 X1
2.5bps

SPI ROM
(4MB)

page 7

SPI BUS
3.3V 33HZ

RTC CKT.
page 30

Touch Screen Control/B
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DC/DC Interface CKT.
page 29

Power Circuit DC/DC
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Power On/Off CKT & Power/B
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AMD FT3 APU

Jaguar Core

Integrated Yangtze FCH

BGA 769-balls

page 5~9

APU SMBus

LPC Bus
3.3V 33 MHz

ENE KB9012
page 27

EC SMBus

Touch Pad
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Int.KBD
page 28

Memory BUS(DDRIII)
Single Channel

1.5V DDRIII 1333/1600 MT/s
APU SMBUS

200pin DDRIII-SO-DIMM X2

BANK 0, 1, 2, 3 page 10, 11

USB 2.0 Left
USB port 0
page 25

TouchScreen
USB port 4
page 20

CardReader
USB port 2
page 20

PCIeMini Card
For BT USB port 1
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USB Right1
USB2.0 port 8
page 24

USB Right2 with S&C
USB2.0 port 9
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Int. Camera
USB port 3
page 20

USB Right1
USB3.0 port 0
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USB Right2
USB3.0 port 1
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SATA Gen3 port 0
5V 6Gbps

SATA HDD
SATA port 0
page 23

HD Audio
3.3V 24MHz

HDA Codec
ALC259
page 26

SPK Conn
page 25

JHP
page 25

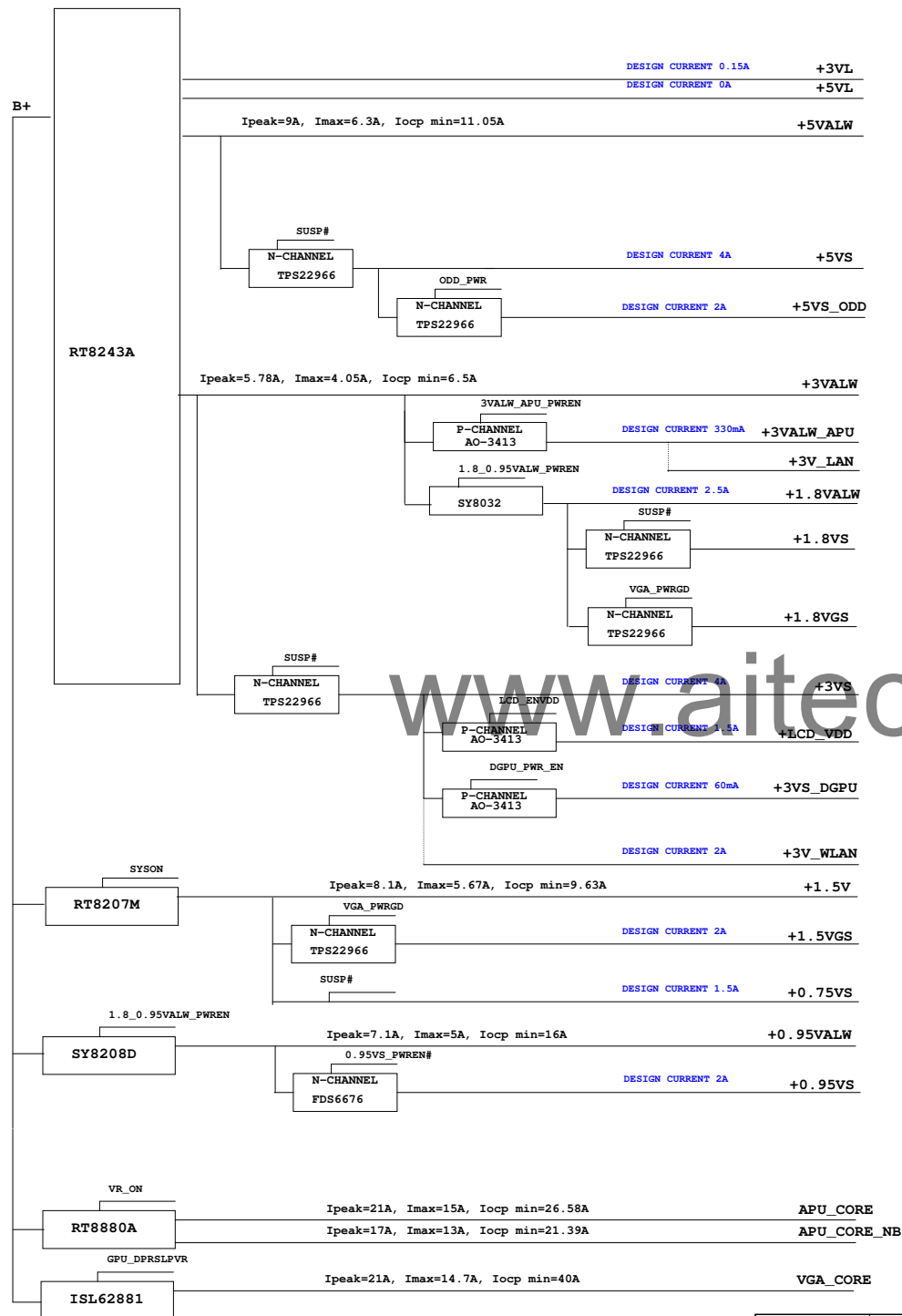
Sub Boards

CardReader GL834L(USB20 port 3)
+USB (USB20 port0)
+Audio Combo jack

page 25

Touch pad/LED B
page 25

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Voltage Rails (O MEANS ON X MEANS OFF)

power plane State	+RTCVCC	B+	+5VL +3VL	+5VALW +3VALW +1.8VALW +0.95VALW +VSB	+1.5V	+5VS +3VS +0.95VS +1.8VS +1.5VS +0.75VS +APU_CORE +APU_CORE_NB
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

UMA BTO Option Table

Function	APU	
description	CPU A4-5000	CPU A6-5200
explain	15W 4C	25W 4C
BTO	A4R1@	A6R1@

Function	GPU	EC			LVDS-eDP		Camera & Mic			KB Light
description	Sun-Pro M2	9012	885		LVDS-eDP		Camera & Mic			KB Light
explain	VGA	9012	w/	w/ EMI	LVDS	eDP	Camera & Mic			KB Light
BTO	VGA@	9012@	885@	885_EMI@	LVDS@	IEDP@	CAM@	CAM@EMI@	@CAM@EMI@	KBL@

Function	LAN	S&C		Size		Codec	Touch Screen	
description	8106E	TI solution		Size		ALC259	Touch Screen	
explain	8106E	TPS2546	TPS2544	14"	15"	ALC259	W/ Touch	W/O EMI Touch
BTO	8106E@	2546@	2544@	14@	15@	259@	Touch_EMI@	@Touch_EMI@

Function	EMI/ESD/RF part				
description	EMI/ESD/RF part				
explain	EMI/ESD/RF part				
BTO	EMI@	@EMI@	ESD@	@ESD@	@RF@

APU SM Bus Address (SCL0/SDA0)

Power	Device	HEX	Address
+3VS	DDR SO-DIMM A	A0H	1010 0000 b
+3VS	DDR SO-DIMM B	A2H	1010 0010 b
+3VS	WLAN		

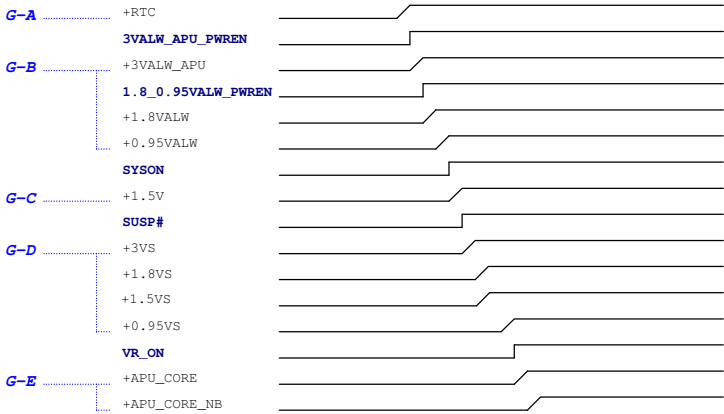
EC SM Bus1 Address

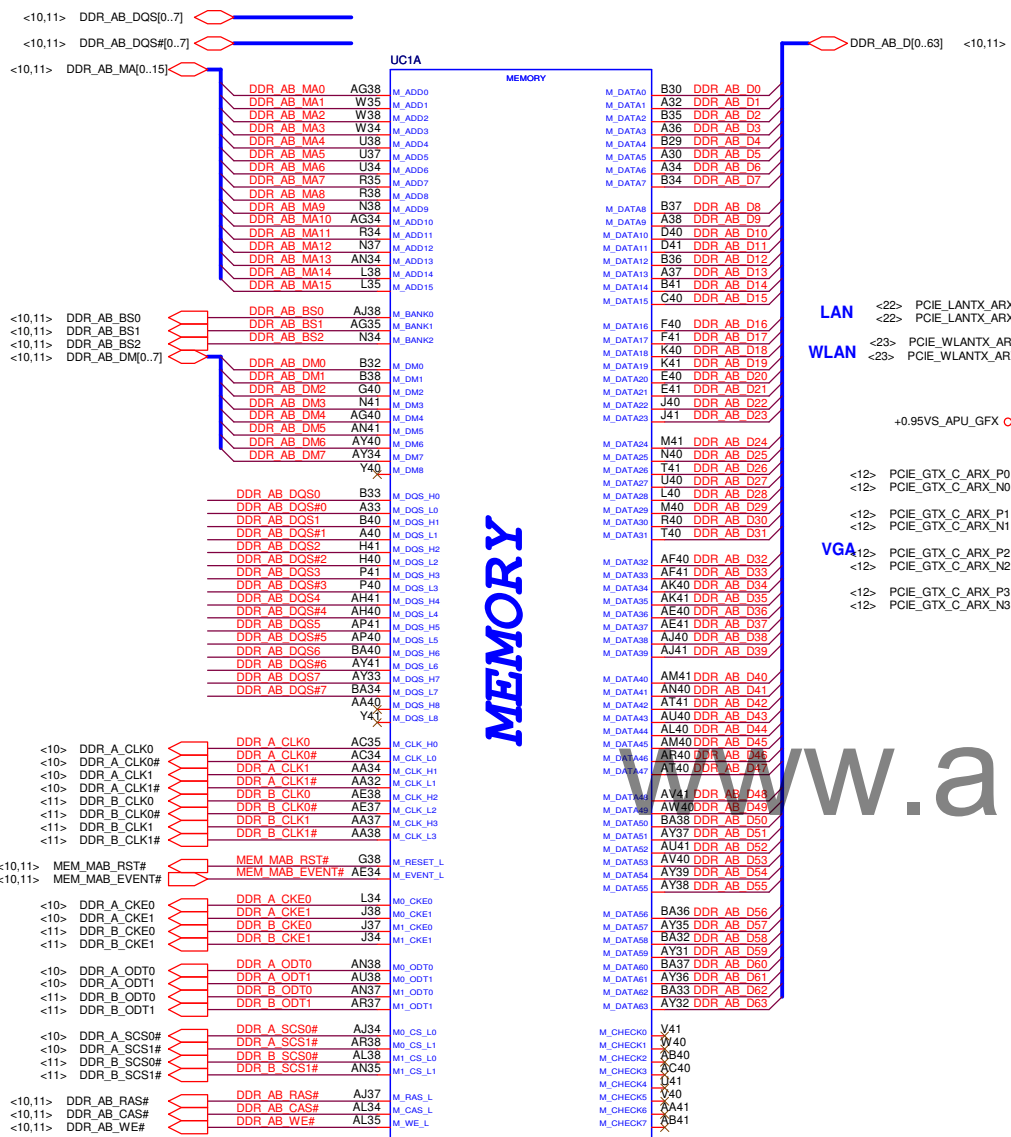
EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Smart Battery	16H	0001 0110 b	+3VS	VGA thermal	82H	1000 0010 b
+3VL	Charger	12H	0001 0010 b	+3VS	APU thermal	98H	1001 1000 b

STATE	SIGNAL	SLP_S3#	SLP_S5#
Full ON		HIGH	HIGH
S1 (Power On Suspend)		HIGH	HIGH
S3 (Suspend to RAM)		LOW	HIGH
S4 (Suspend to Disk)		LOW	HIGH
S5 (Soft OFF)		LOW	LOW
G3		LOW	LOW

APU POWER SEQUENCE

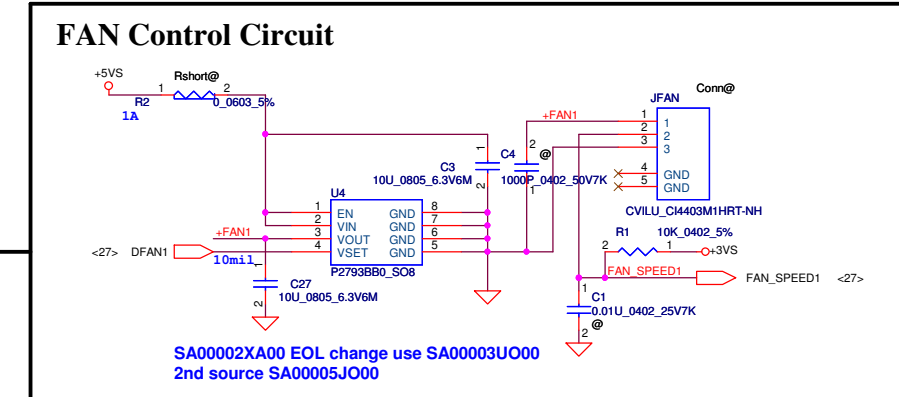




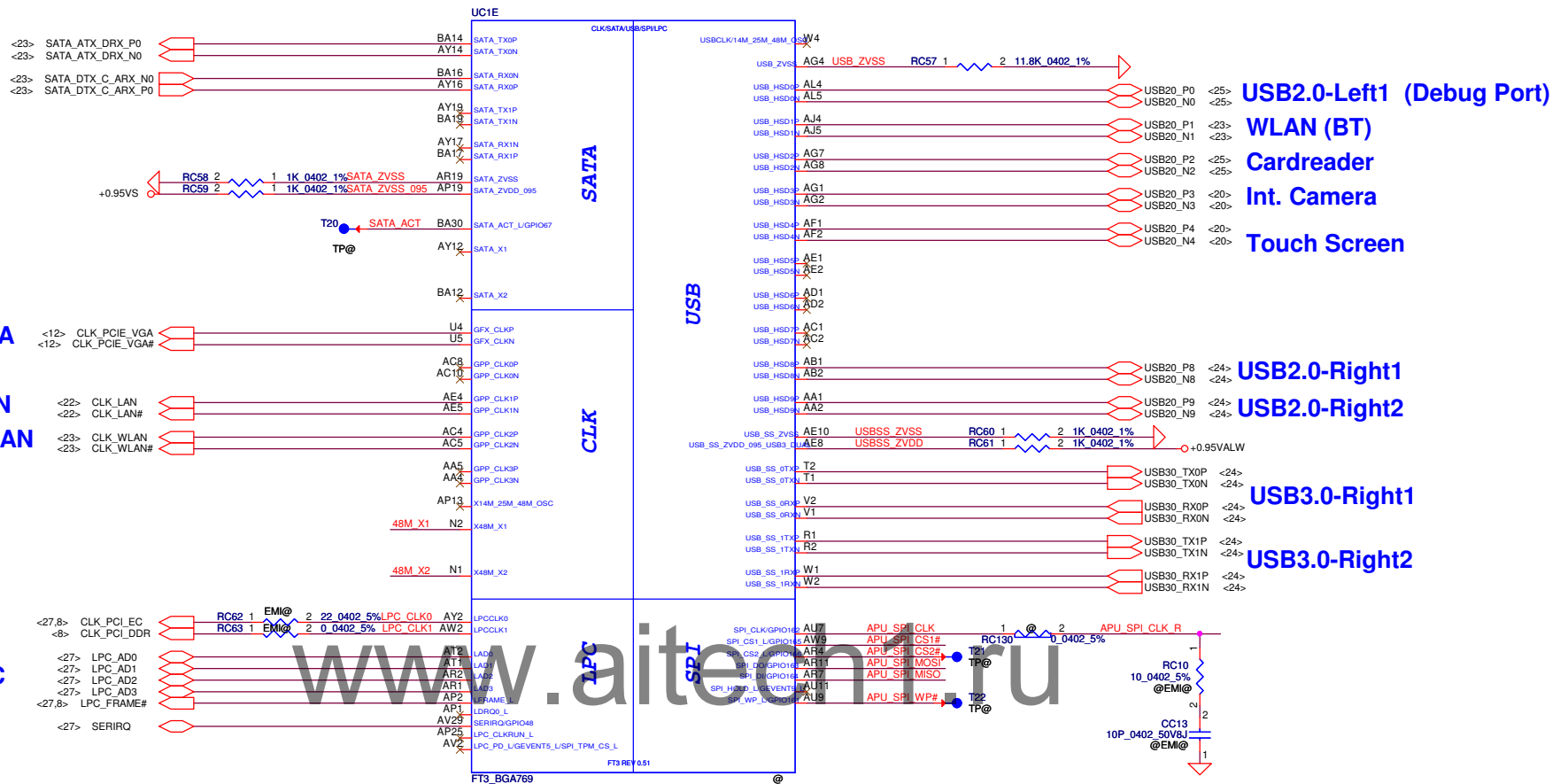
MEMORY

GRAPHICS

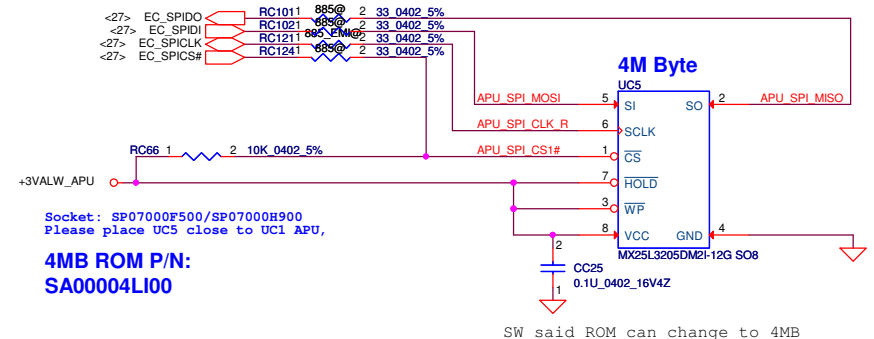
GPP



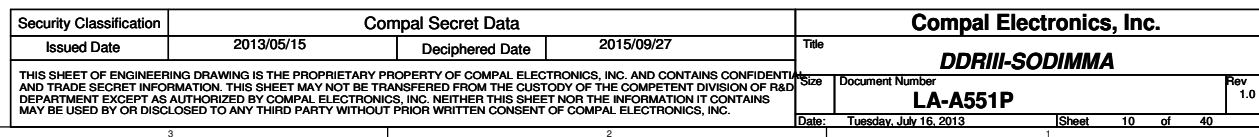
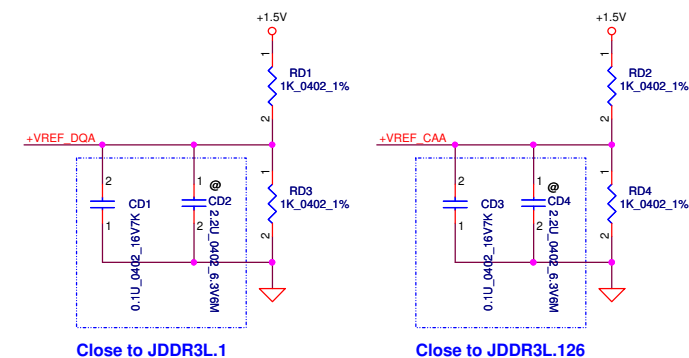
Security Classification		Compal Secret Data		Title	
Issued Date	2013/05/15	Deciphered Date	2015/09/27	FT3 DISP/MISC/HDT	
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The schematic diagram shows a 48MHz oscillator circuit. It features a 48MHz crystal (YC1, 48MHZ_8PF_X3S048000D81H-W) connected to a 48MHz buffer (1M_0402_5%). The buffer is connected to two 48MHz input/output lines (X1 and X2). The circuit also includes two capacitors (CC22 and CC23, 4.7P_0402_50VB) connected to ground.



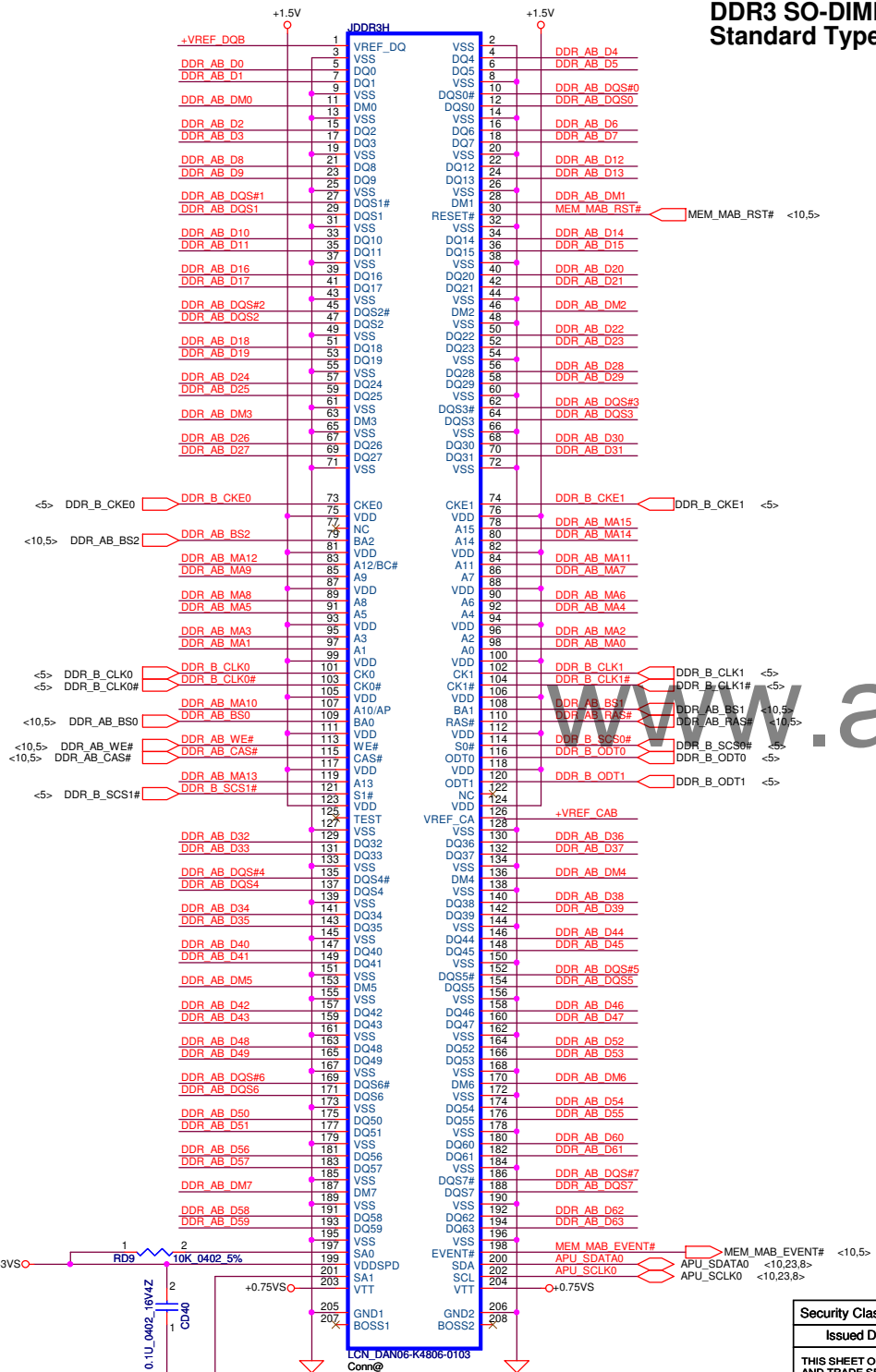
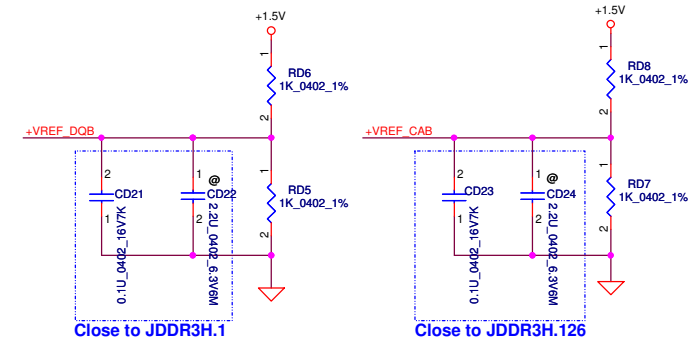
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DDR3 SO-DIMM B Standard Type

DDR_AB_DQS[0..7] <10,5>
DDR_AB_DQS[0..7] <10,5>
DDR_AB_D[0..63] <10,5>
DDR_AB_DM[0..7] <10,5>
DDR_AB_MA[0..15] <10,5>

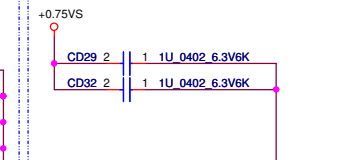
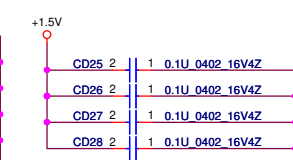
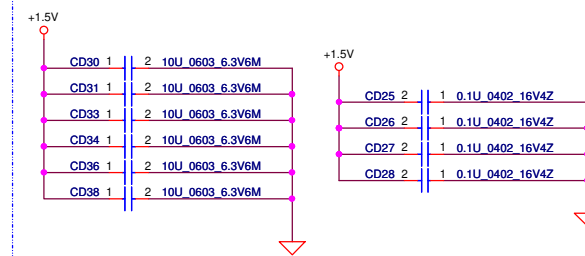
SO-DIMM VREF



Layout Note:
Place near JDDR3H

Layout Note: Place these 4 Caps near
Command and Control signals of DIMMB

Layout Note:
Place near JDDRH.203 and 204



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<5> PCIE_ATX_C_GRX_P[3..0] PCIE_ATX_C_GRX_P[3..0]
<5> PCIE_ATX_C_GRX_N[3..0] PCIE_ATX_C_GRX_N[3..0]

UV1A

PART 1 OF 9

PCIE GTX_C_ARX_P[3..0] PCIE GTX_C_ARX_P[3..0]
PCIE GTX_C_ARX_N[3..0] PCIE GTX_C_ARX_N[3..0]

PCIE GTX_C_ARX_P[3..0] PCIE GTX_C_ARX_P[3..0]
PCIE GTX_C_ARX_N[3..0] PCIE GTX_C_ARX_N[3..0]

LVDS Interface

UV1D

PART 7 OF 9

RSVD/VARY BL
RSVD/DIGON

LVDS CONTROL

TXCBP_DPB3P
TXCBM_DPB3N

TX3P_DPB2P
TX3M_DPB2N

TX4P_DPB1P
TX4M_DPB1N

TX5P_DPB0P
TX5M_DPB0N

NC#AF35
NC#AG36

TXCAP_DPA3P
TXCAM_DPA3N

TX0P_DPA2P
TX0M_DPA2N

TX1P_DPA1P
TX1M_DPA1N

TX2P_DPA0P
TX2M_DPA0N

NC
NC

VGA@ SUN-PRO M2_FCBGA962

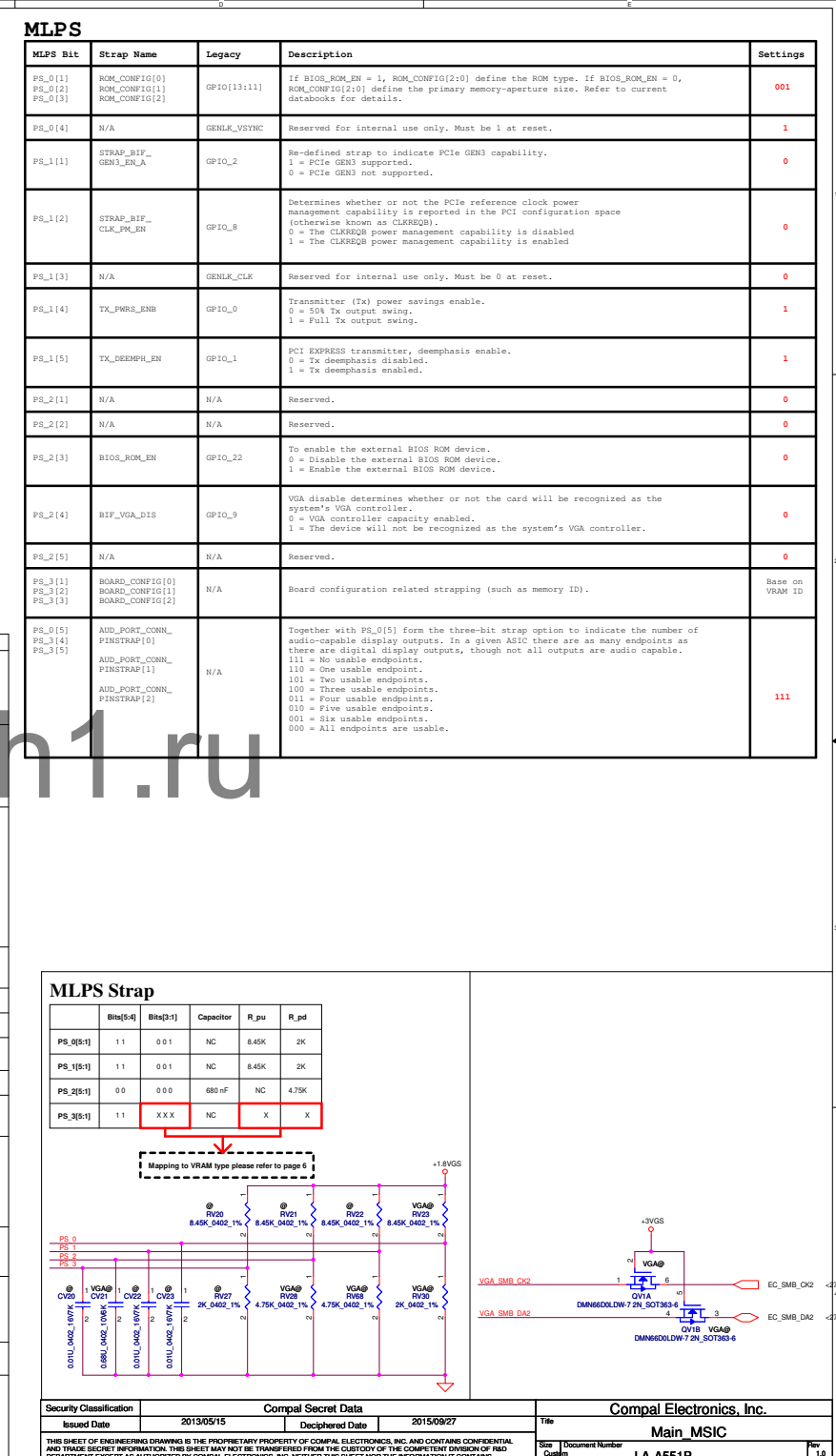
AC Coupling Capacitor
PCIeR Gen1 and Gen2 only: Recommended value is 100 nF 10%.
PCIeR Gen3: Recommended value is 220 nF 10%.

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For MEMCLK 1GHz	Brand	Description	Comment	PS_3[3:1]	R_pu(ohm)	R_pd(ohm)
gDDR3-2Gbit	skHynix	H5TQ2G63DFR-N0C	1.5V/1GHz	000	NC	4750
	Samsung	K4W2G1646E-BC1A	1.5V/1GHz	111	4750	NC

For MEMCLK 900MHz	Brand	Description	Comment	PS_3[3:1]	R_pu(ohm)	R_pd(ohm)
gDDR3-2Gbit	skHynix	H5TQ2G63DFR-11C	1.5V/900MHz	000	NC	4750
	Micron	MT41K128M16JT-107G:K	1.35V/900MHz 1.5V/900MHz	001	8450	2000
	Samsung	K4W2G1646E-BC11	1.5V/900MHz	111	4750	NC

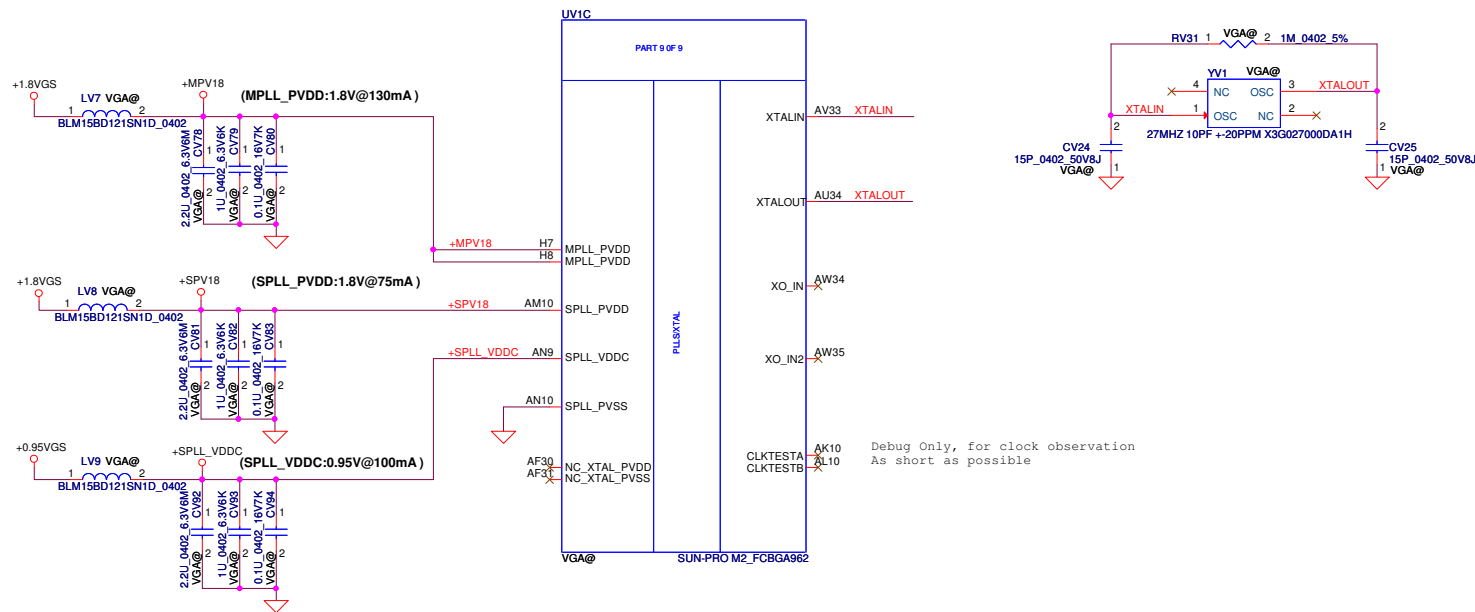
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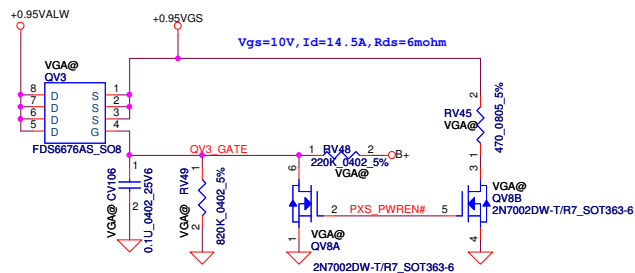
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
2.2u	1	1

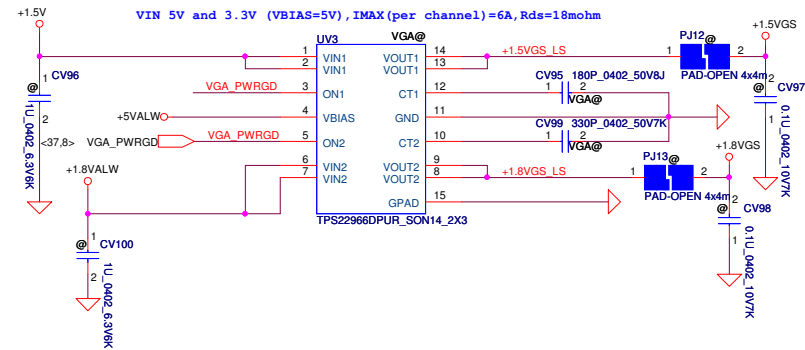


+0.95VS to +0.95VGS



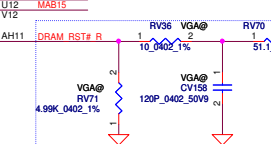
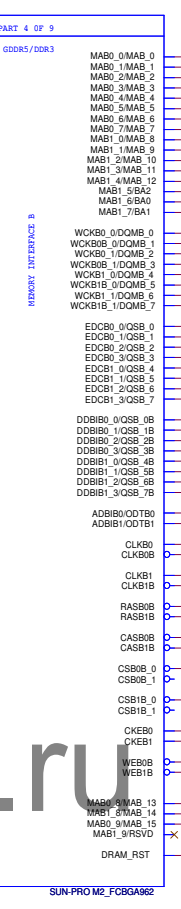
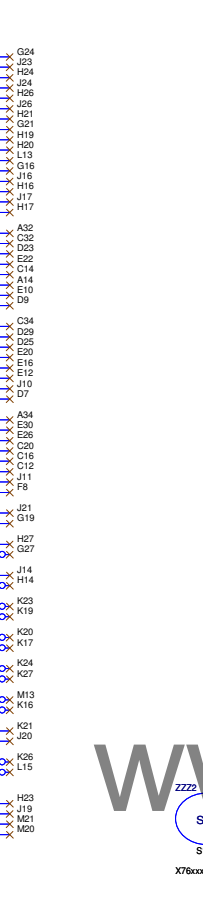
Only for Kabini

+1.8VALW to +1.8VGS
+1.5V to +1.5VGS



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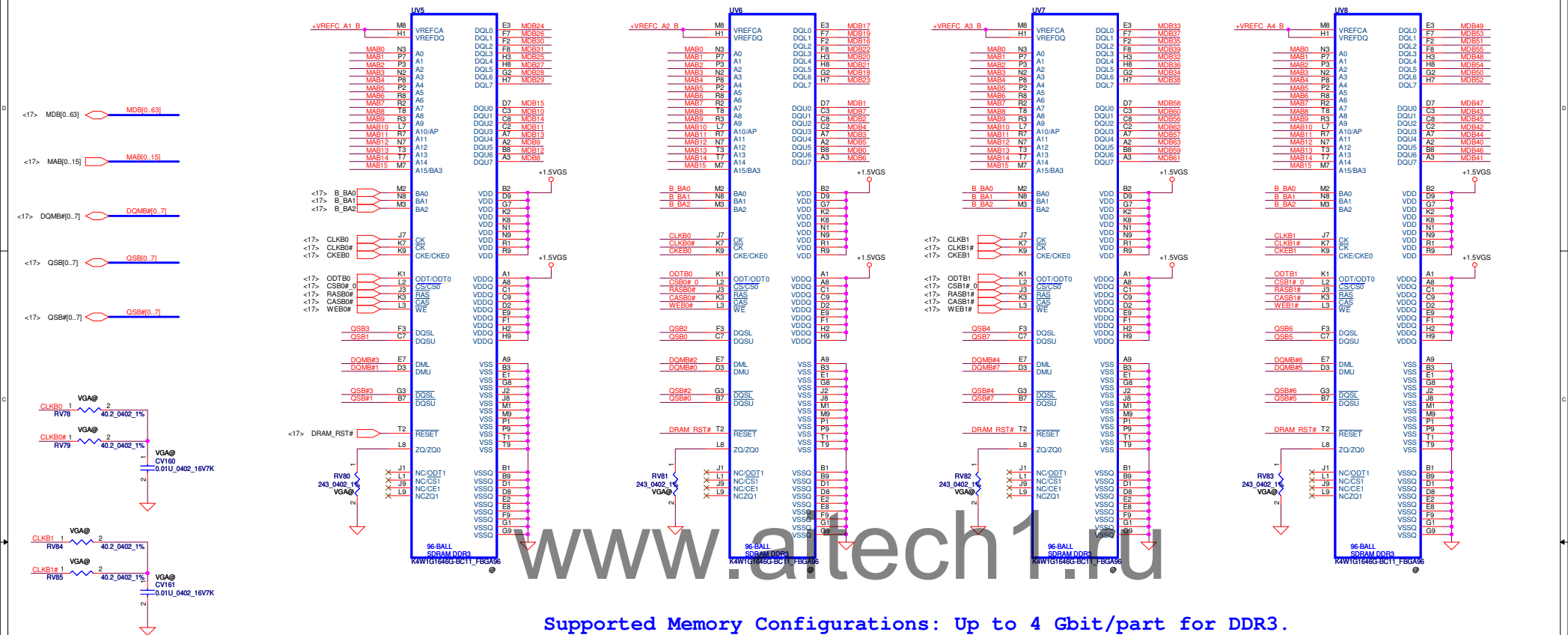
R_{pu} & R_{pd} resistor:
0402 1% resistors are required.

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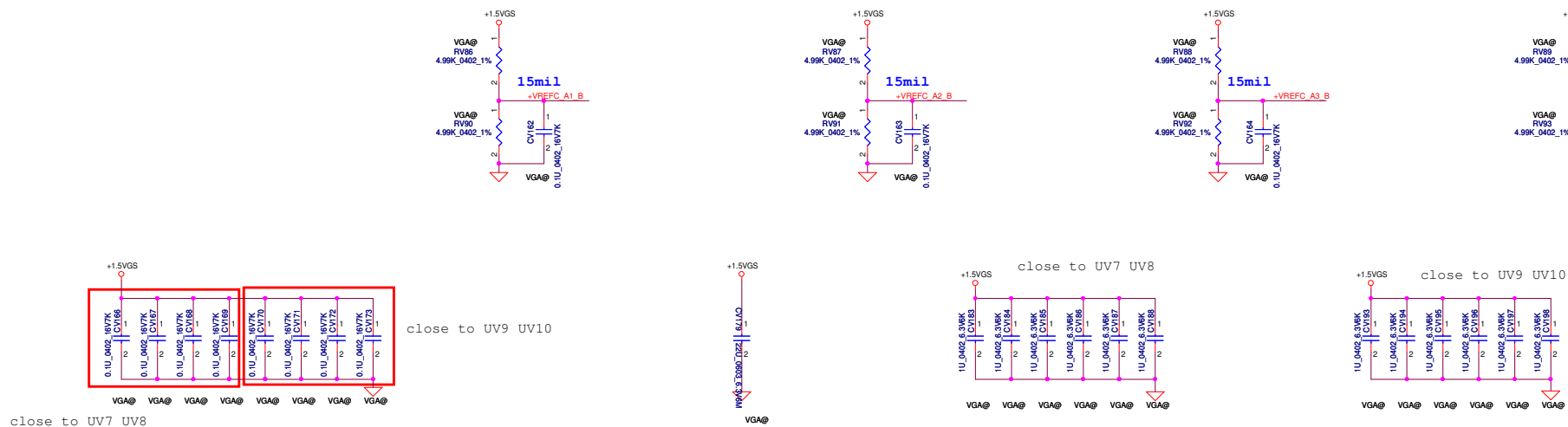


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CHANNEL B: 512MB/1024MB DDR3



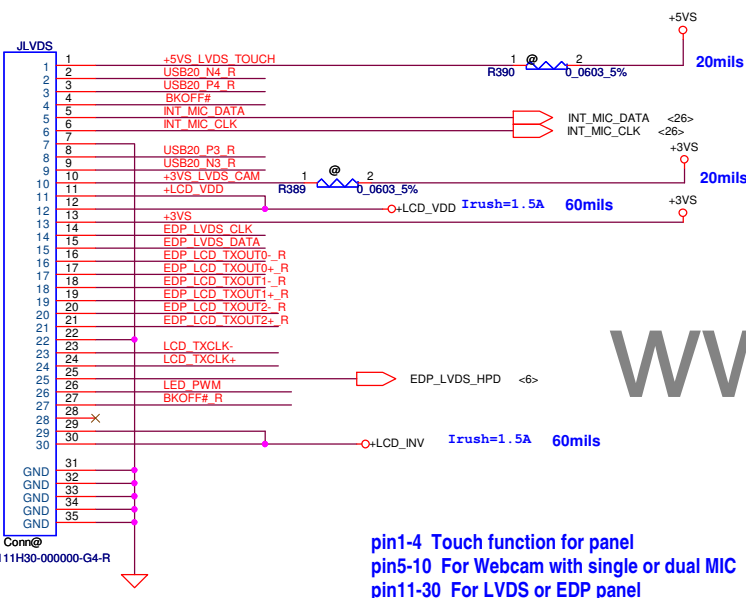
Supported Memory Configurations: Up to 4 Gbit/part for DDR3.



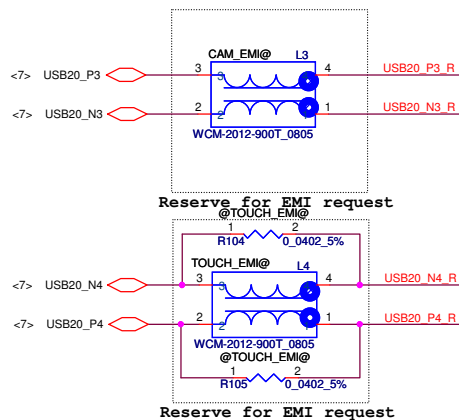
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<6> EDP_LCD_TXOUT0+_R EDP_LCD_TXOUT0+_R
 <6> EDP_LCD_TXOUT0-_R EDP_LCD_TXOUT0-_R
 <6> EDP_LCD_TXOUT1+_R EDP_LCD_TXOUT1+_R
 <6> EDP_LCD_TXOUT1-_R EDP_LCD_TXOUT1-_R
 <6> EDP_LCD_TXOUT2+_R EDP_LCD_TXOUT2+_R
 <6> EDP_LCD_TXOUT2-_R EDP_LCD_TXOUT2-_R
 <6> LCD_TXCLK+ LCD_TXCLK+
 <6> LCD_TXCLK- LCD_TXCLK-
 <6> EDP_LVDS_CLK EDP_LVDS_CLK
 <6> EDP_LVDS_DATA EDP_LVDS_DATA

If it's EPD, they're become
 LCD_TXOUT2+_R = EDP_TX0+
 LCD_TXOUT2-_R = EDP_TX0-
 LCD_TXOUT1+_R = EDP_TX1+
 LCD_TXOUT1-_R = EDP_TX1-
 LVDS_CLK = EDP_AUXP
 LVDS_DATA = EDP_AUXN

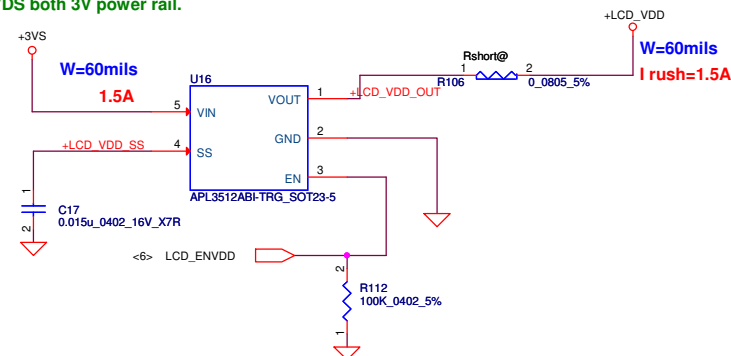


Camera & Touch Screen

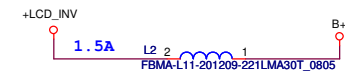
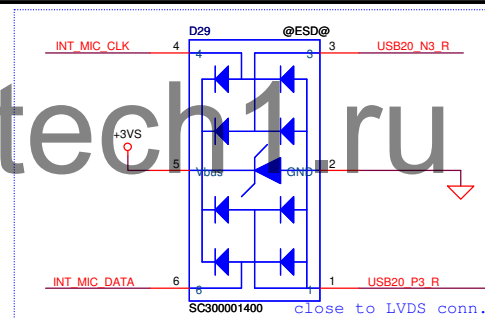


LCD_VDD

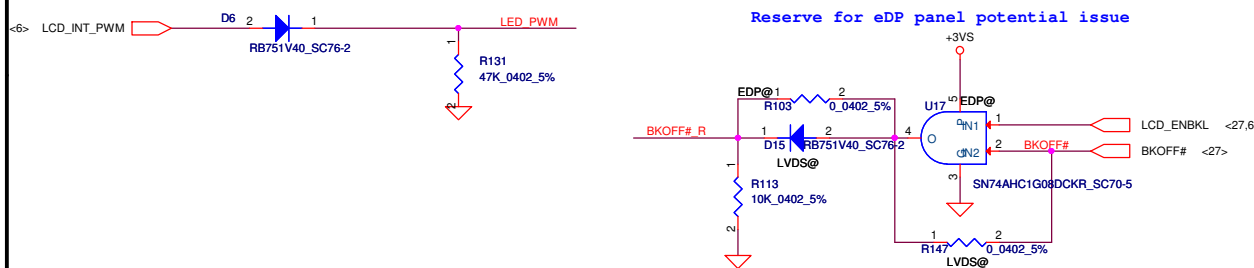
Need check eDP&LVDS both 3V power rail.



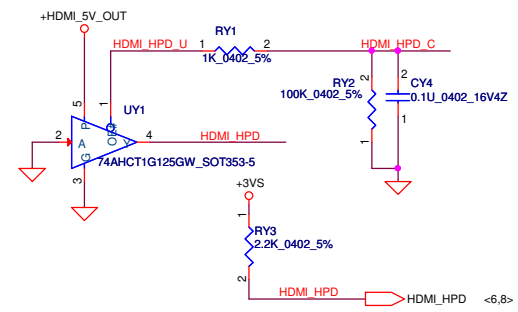
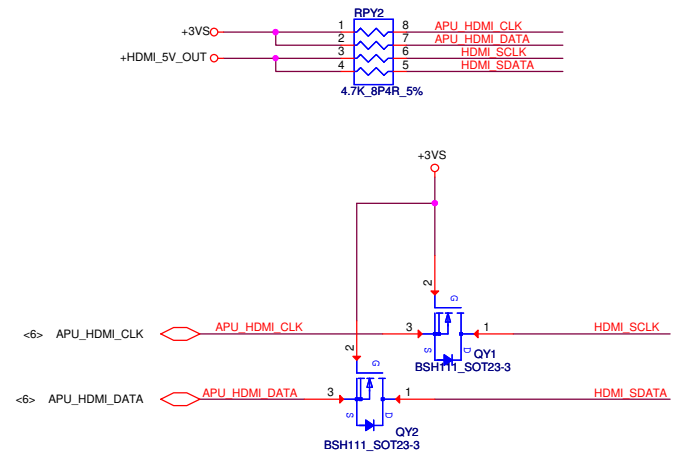
LCD_INV



LCD Control



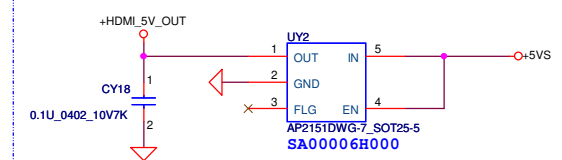
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2013/05/15	Deciphered Date	2015/09/27	Title	LVDS/EDP W/ CAMERA	
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					LA-A551P	0.2
				Date	Tuesday, July 16, 2013	Sheet 20 of 40



OE#	A	Y
L	L	L
L	H	H
H	X	Z

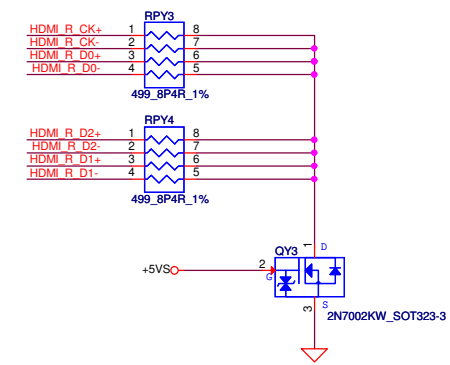
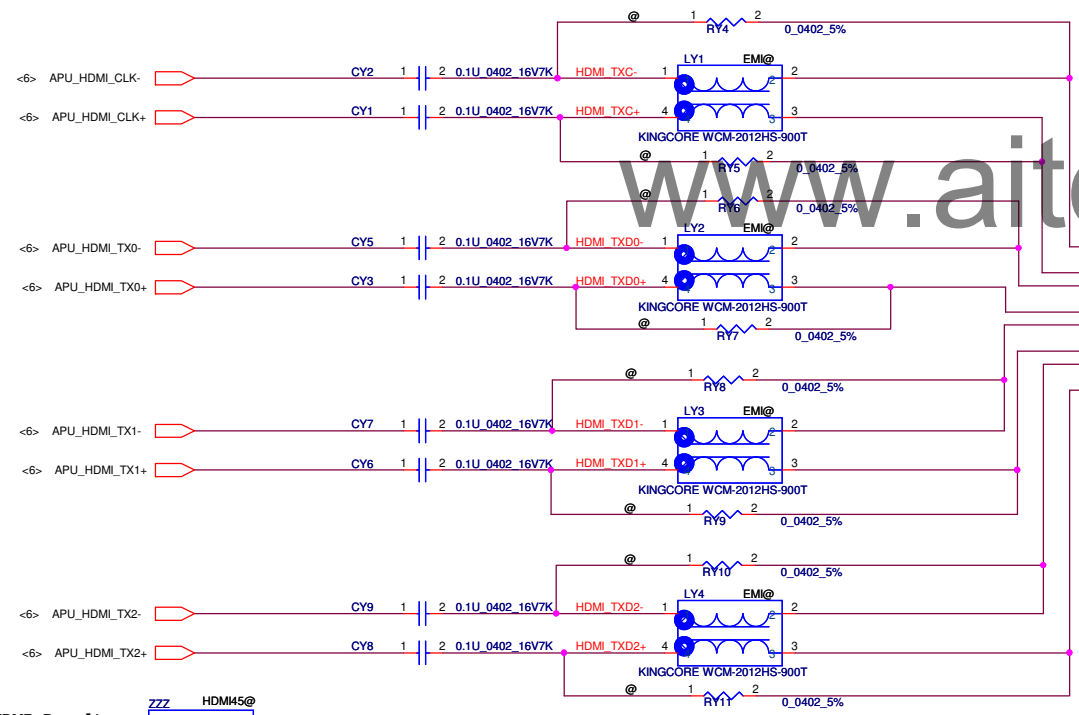
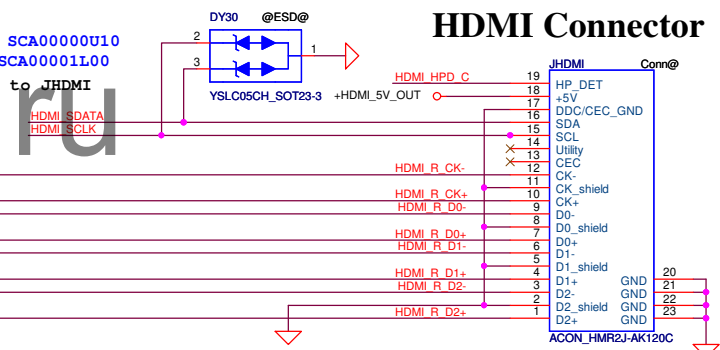
HDMI POWER CIRCUIT

VIN = 5V, IOUT = 0.5A , RDS(ON) TYP=95m ; MAX=115m
Current Limit: TYP=0.8A ; MAX=1A



HDMI Connector

Main: SCA00000U10
2nd: SCA00001L00
Close to JHDMI

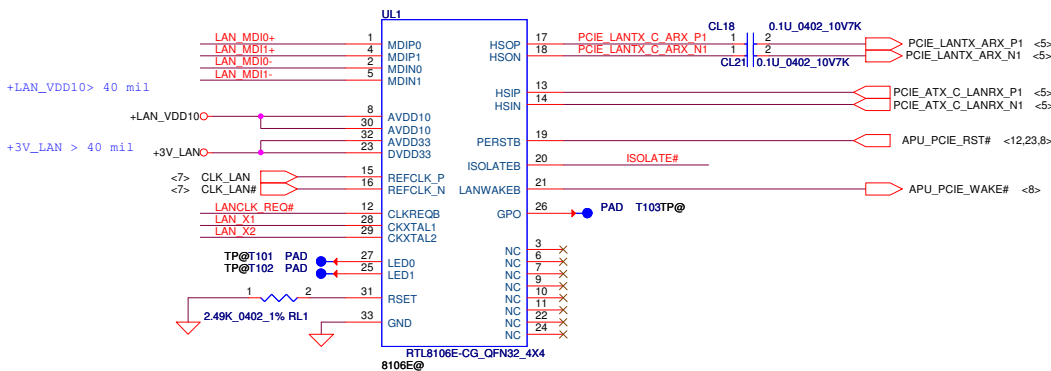


HDMI Royalty
HDMI45@
RO0000003HMM
HDMI W/Logo + HDCP

HDMI W/O Logo: RO0000001HMM
HDMI W/Logo: RO0000002HMM
HDMI W/Logo + HDCP: RO0000003HMM

please manually load
this virtual material to 45@ BOM

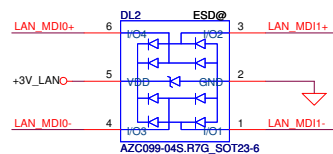
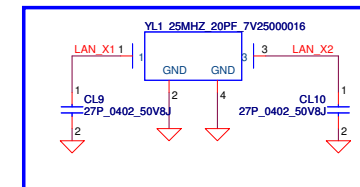
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2013/05/15		Deciphered Date		2015/09/27		Title	
										HDMI W/O CEC	
										LA-A551P	
										Date: Tuesday, July 16, 2013	
										Sheet 21 of 40	



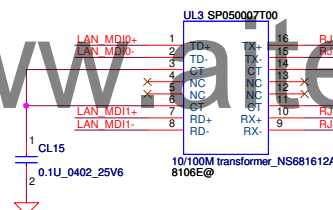
CL2, CL4 close to pin 8, 30 respectively
CL6 close to pin 30

CL8 close to Pin32
CL20 close to Pin23

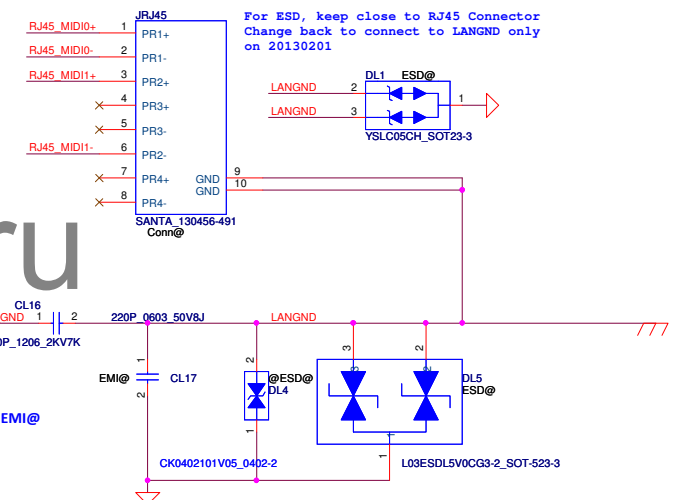
Keep de-coupling capacitors close to RTL8106E within 200 mil



main: SP050007T00
2nd: SP050007K00
3rd: SP050006H00



For ESD, keep close to RJ45 Connector
Change back to connect to LANGND only on 20130201



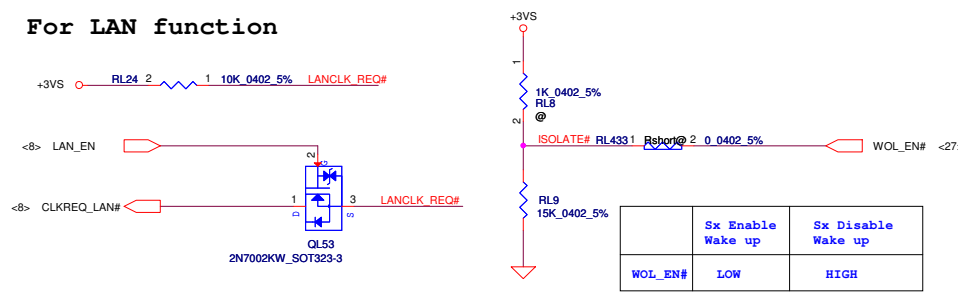
2013/5/3 EMI request change CL17 BOM structure to EMI@
2013/6/7 ESD request reserve DL14
2013/6/7 ESD request add DL5

LAN	WOL	LAN_EN		ISOLATEB	
		S0	Sx	S0	Sx
0	0	0	0	1	1
0	1	0	0	1	1
1	0	1	1	1	1
1	1	1	1	1	0*

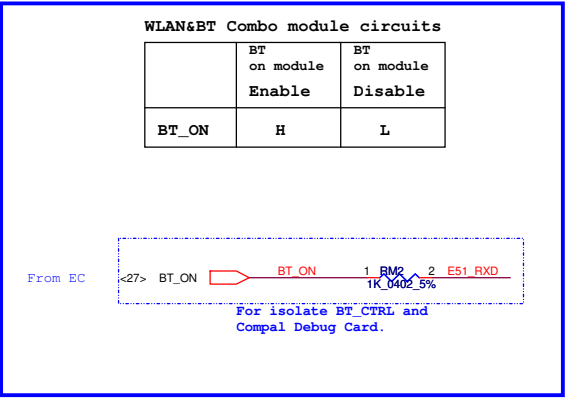
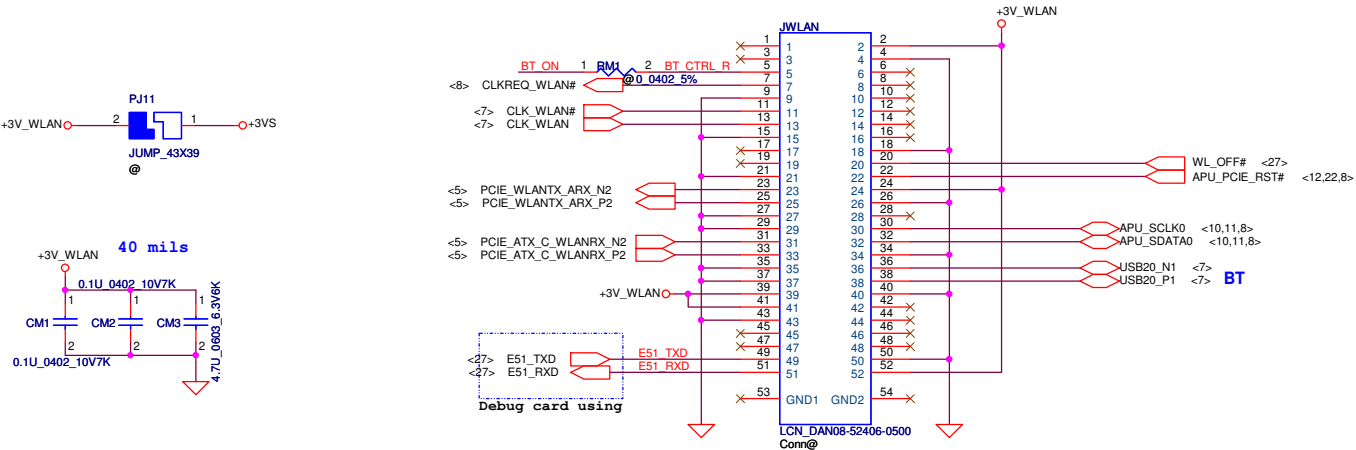
*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

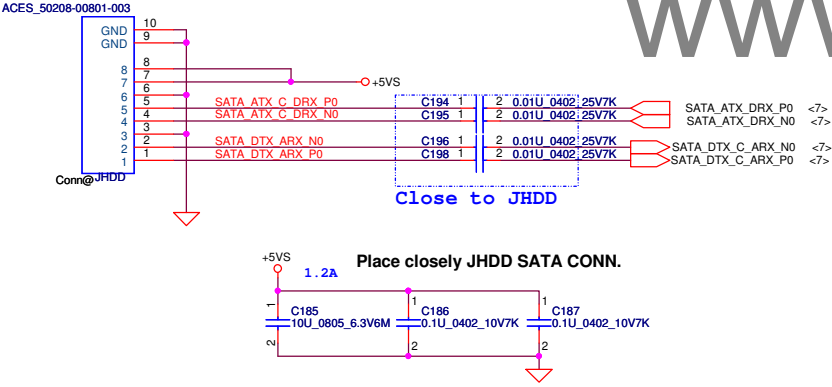
For LAN function



Slot 1 Half PCIe Mini Card-WLAN



SATA HDD Conn.

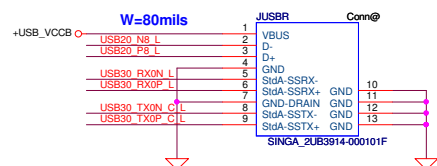
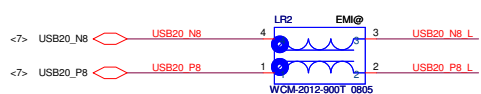
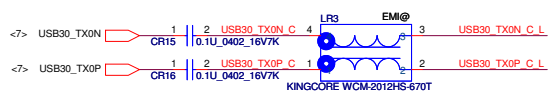


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State table for TPS2546RTER

CB0	CB1	CB2	ILIM_SEL	Mode	STATUS
0	1	1	1	Auto/Alternate	Auto-detection charger mode for Apple device(2A,1A). Resistor dividers are connected to DP/DM. Including DCP
1	1	1	0	SDP	USB pass-through mode.DP/DM are connected to TDP/TDM
1	1	1	1	CDP	USB pass-through mode with CDP emulation. DP/DM are connected to TDP/TDM

Timing diagram for USB3 RX0N and RX0P signals. The diagram shows two input signals, USB3_RX0N and USB3_RX0P, and their corresponding outputs, USB3_RX0N_L and USB3_RX0P_L. The outputs are shown as blue waveforms with a period of 100ns. The diagram is labeled 'KINGCORE WCM-2012HS-670T'.



2.0A

W=60mils

+5VALW

+USB_VCCB

UR2

2 **3** **4** **5** **6** **8**

IN **OUT** **EN/ENB** **GND** **OCB**

<27> **USB_EN#0** **USB_OC#0** **<27,S>**

SY6288DCAC_MSOP8

SA00003TV00

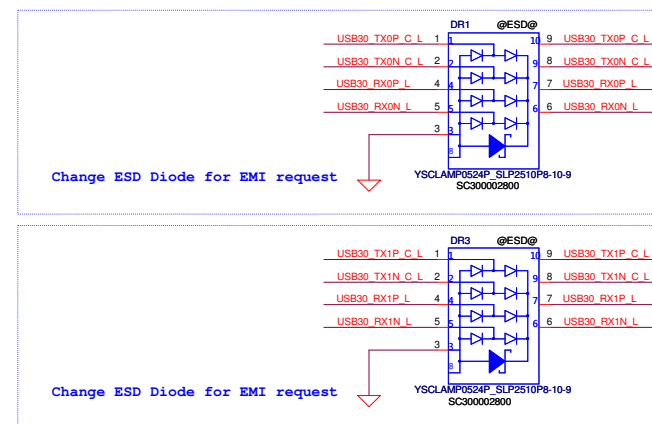
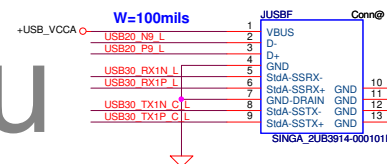
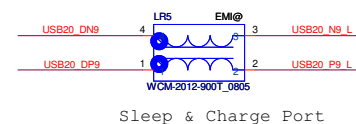
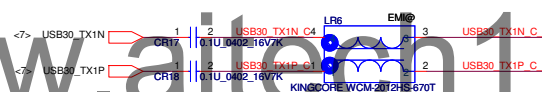
SA00003XM00

+USB_VCCB

W=80mils

CR11 **CR13** **CR6** **CR10**

0.1u 0402_1W7K **7U_0603_6.3V6A** **22uJ_0603_6.3V6M** **22uJ_0603_6.3V6M**

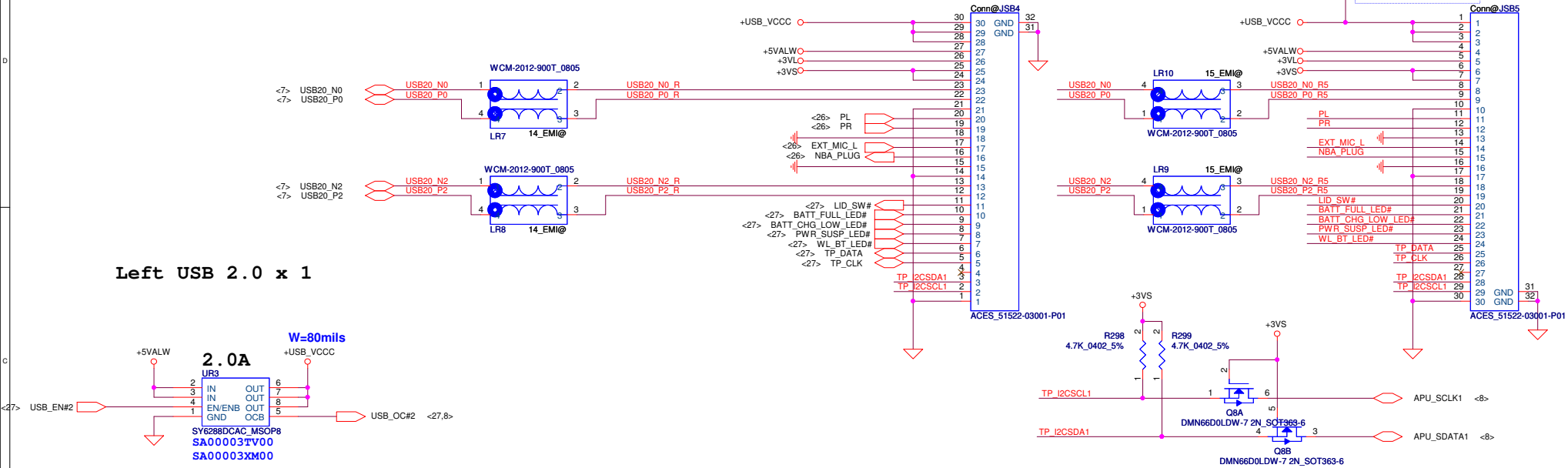
[illegible]

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					USB/RUSB/S&C
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Small board Conn

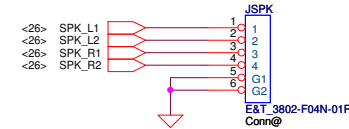
Close to JSB5

Left USB 2.0 x 1

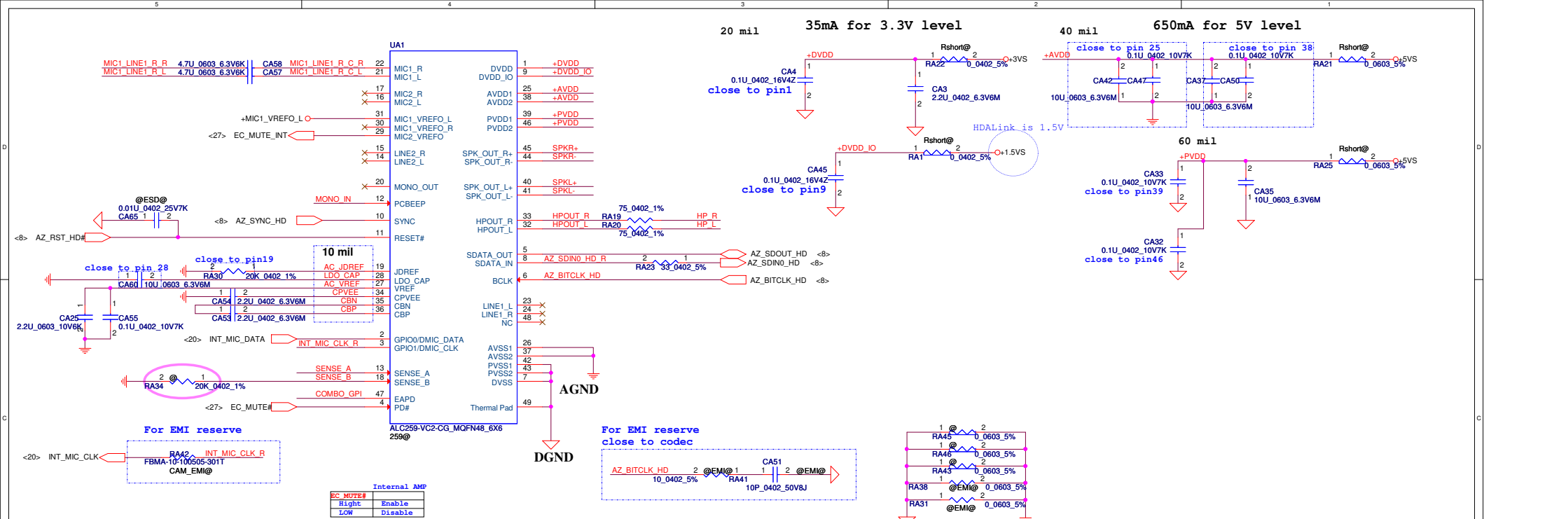


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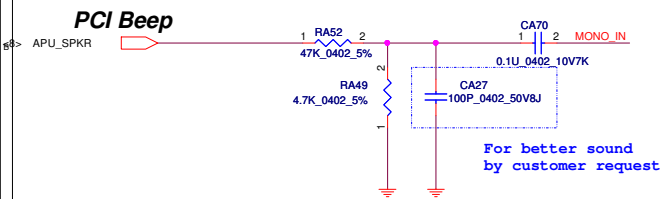
SPK Conn.



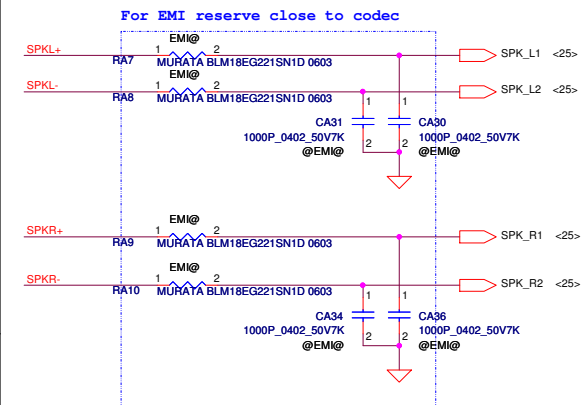
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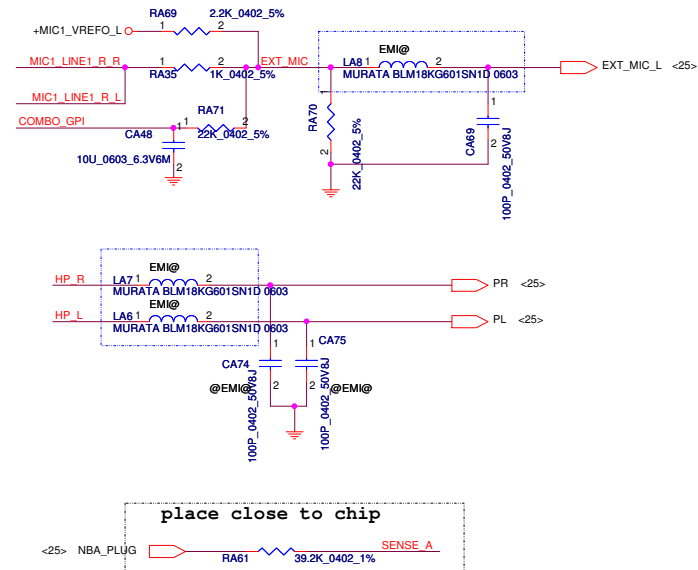
Beep sound



SPK 2W 4ohm =40mil
1W 8ohm =20mil



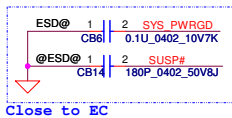
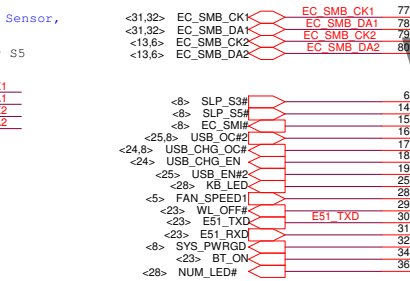
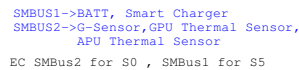
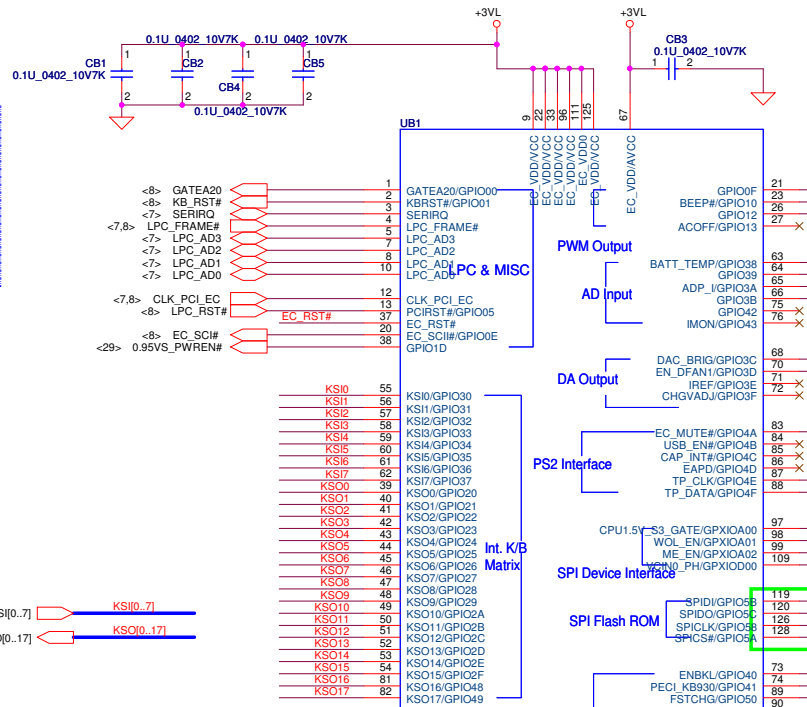
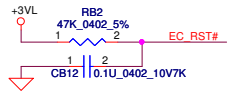
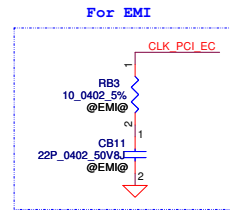
Combo Jack



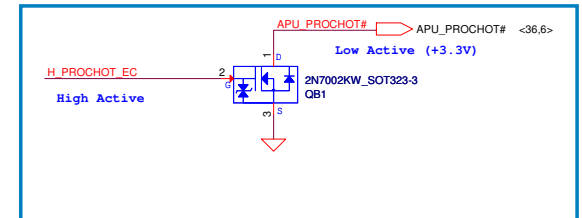
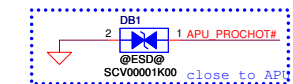
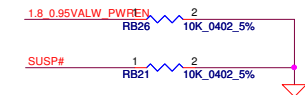
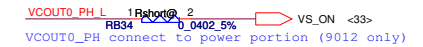
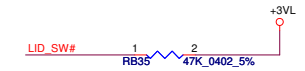
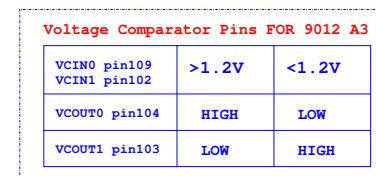
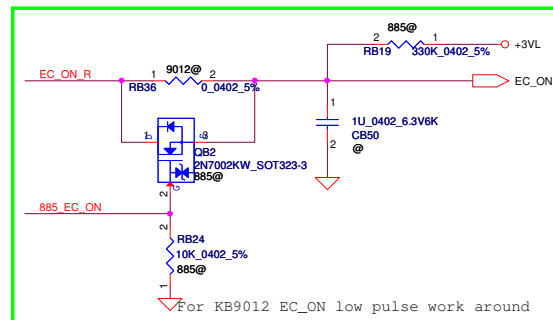
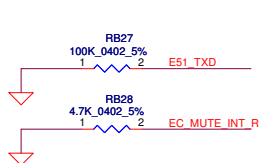
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 20)	

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20130417 Note. 2013 ENE EC change version
A3 (SA000040B20) to A4 (SA000040B30)

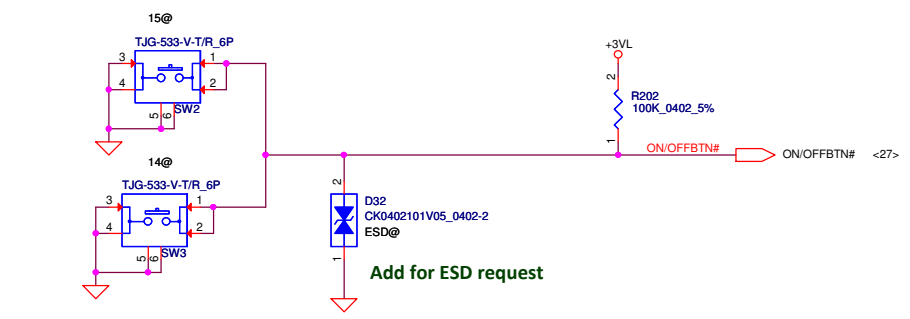


P.32_SYS_PWRGD OD/L
for 1.8V PU APU

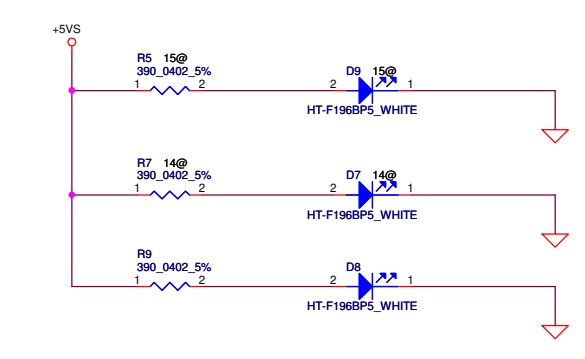


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				LPC-EC-KB9012	
				Document Number	
				LA-A551P	
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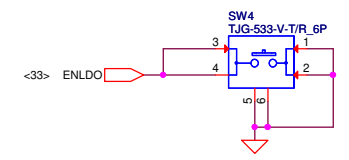
Power Button



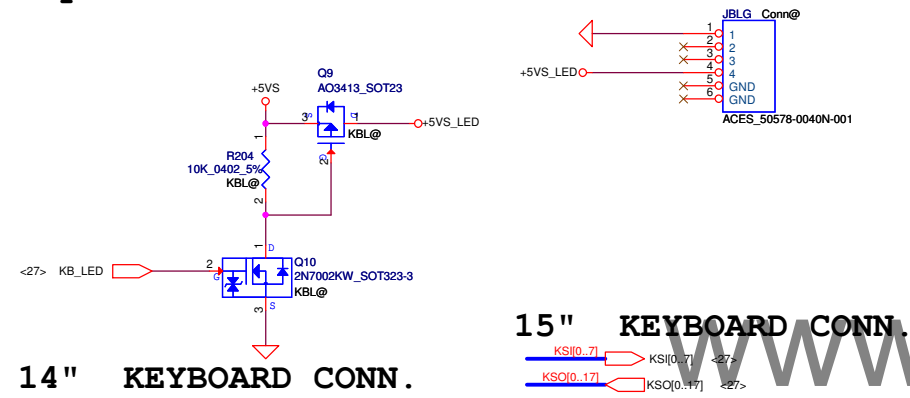
POWER LED



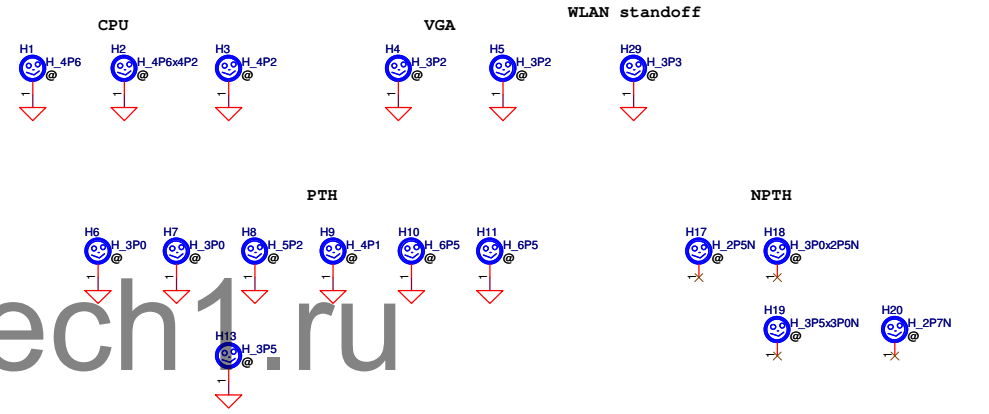
Battery Reset



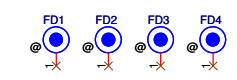
Keyboard LED



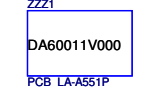
Screw Hole



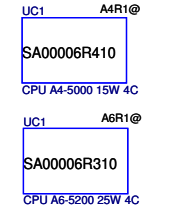
PCB Fedical Mark PAD



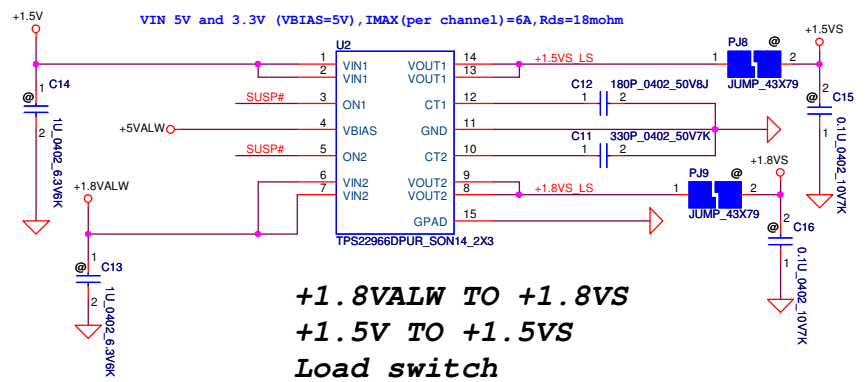
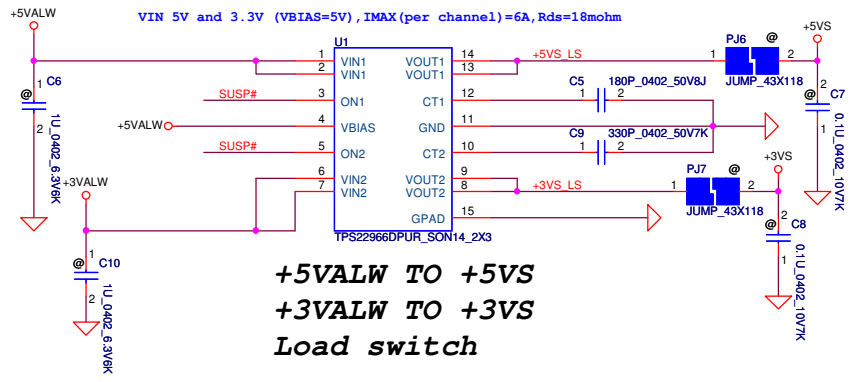
ISPD



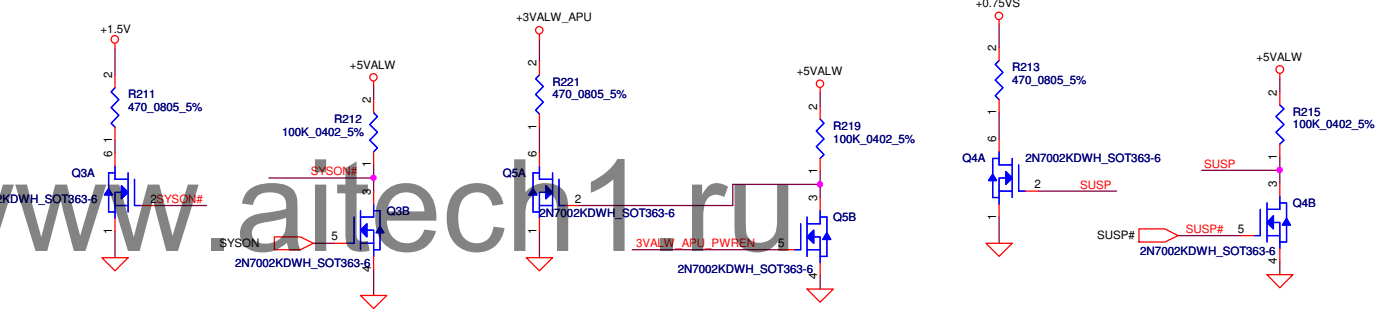
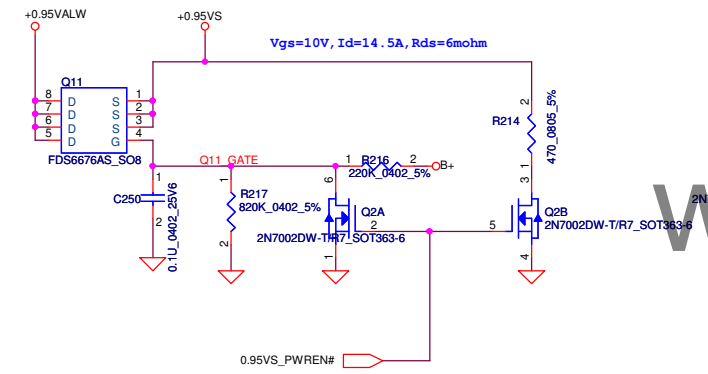
APU PR sample



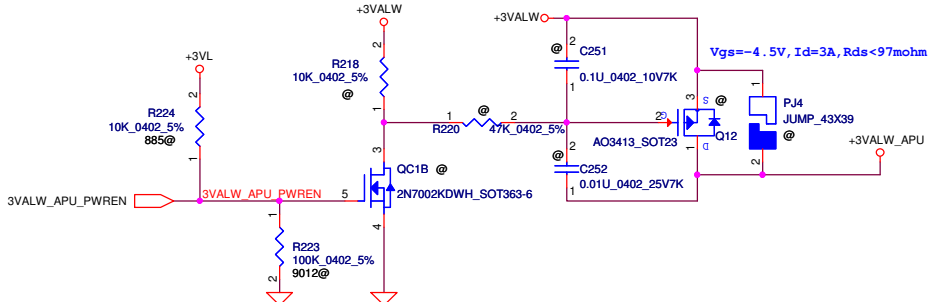
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				Size	Document Number
				LA-A551P	
				Date	Rev
				Tuesday, July 16, 2013	1.0
				Sheet	28 of 40



+0.95VALW to +0.95VS



+3VALW to +3VALW_FCH

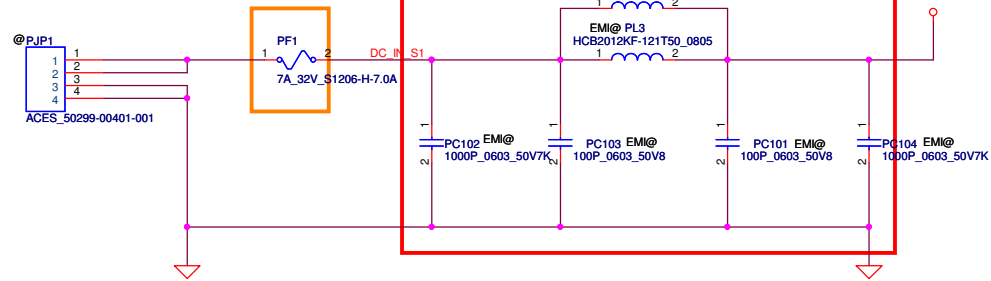


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				Date	Tuesday, July 16, 2013
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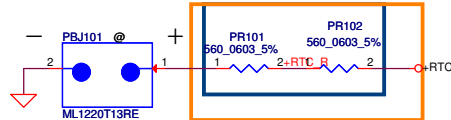
EMI Part (47.1)

Other component (37.1)

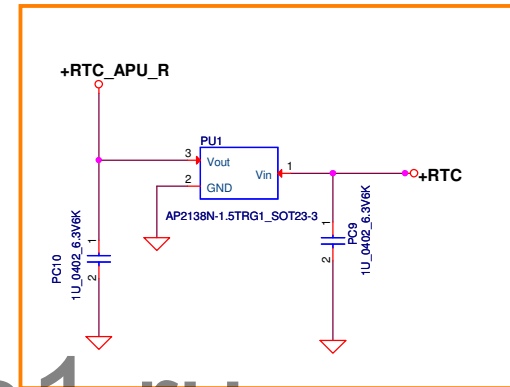
A51 need add fuse



For ML1220 RTC (38.2)

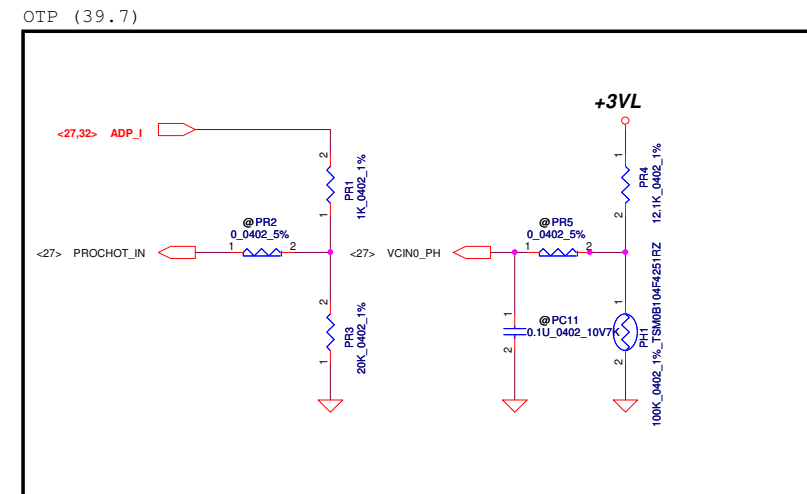
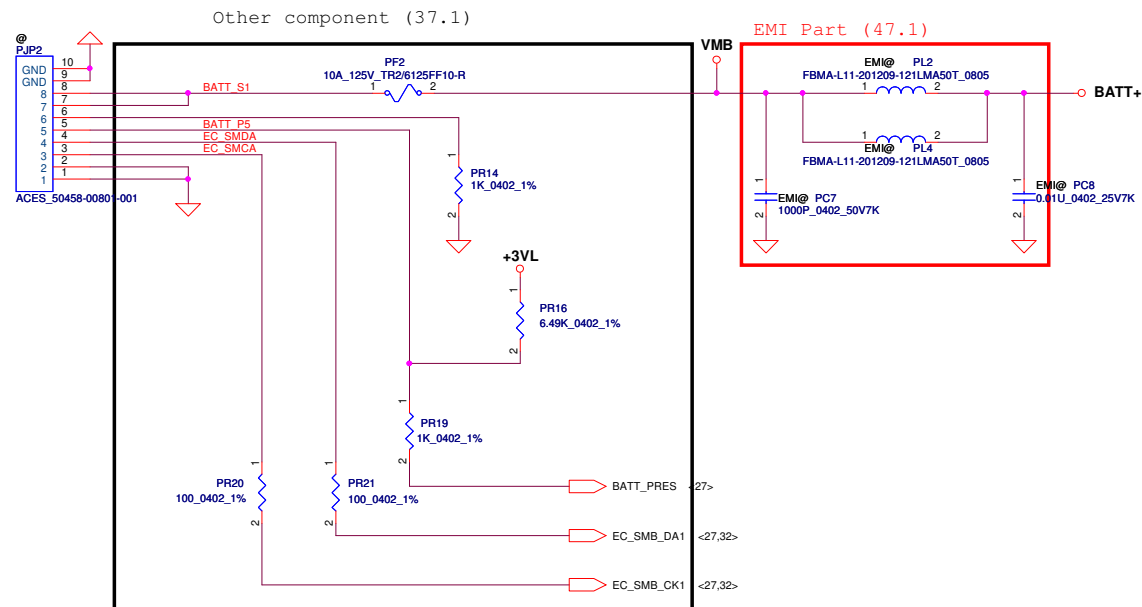


For RTC (38.2)



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				Date:	Rev 0.1
				Sheet	30 of 40

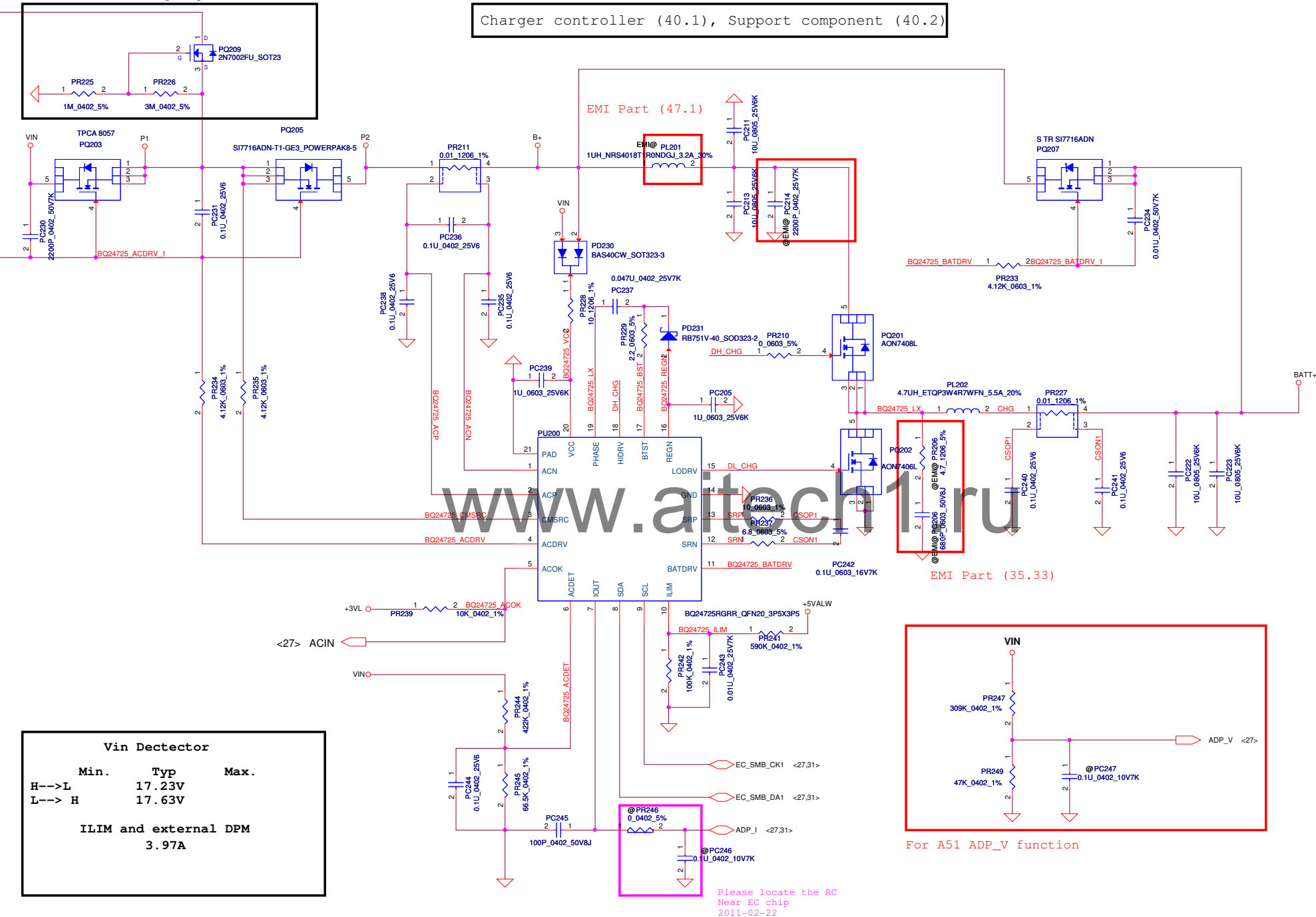


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				Document Number	LA-A551P
				Date:	Rev 0.1
				Sheet	31 of 40

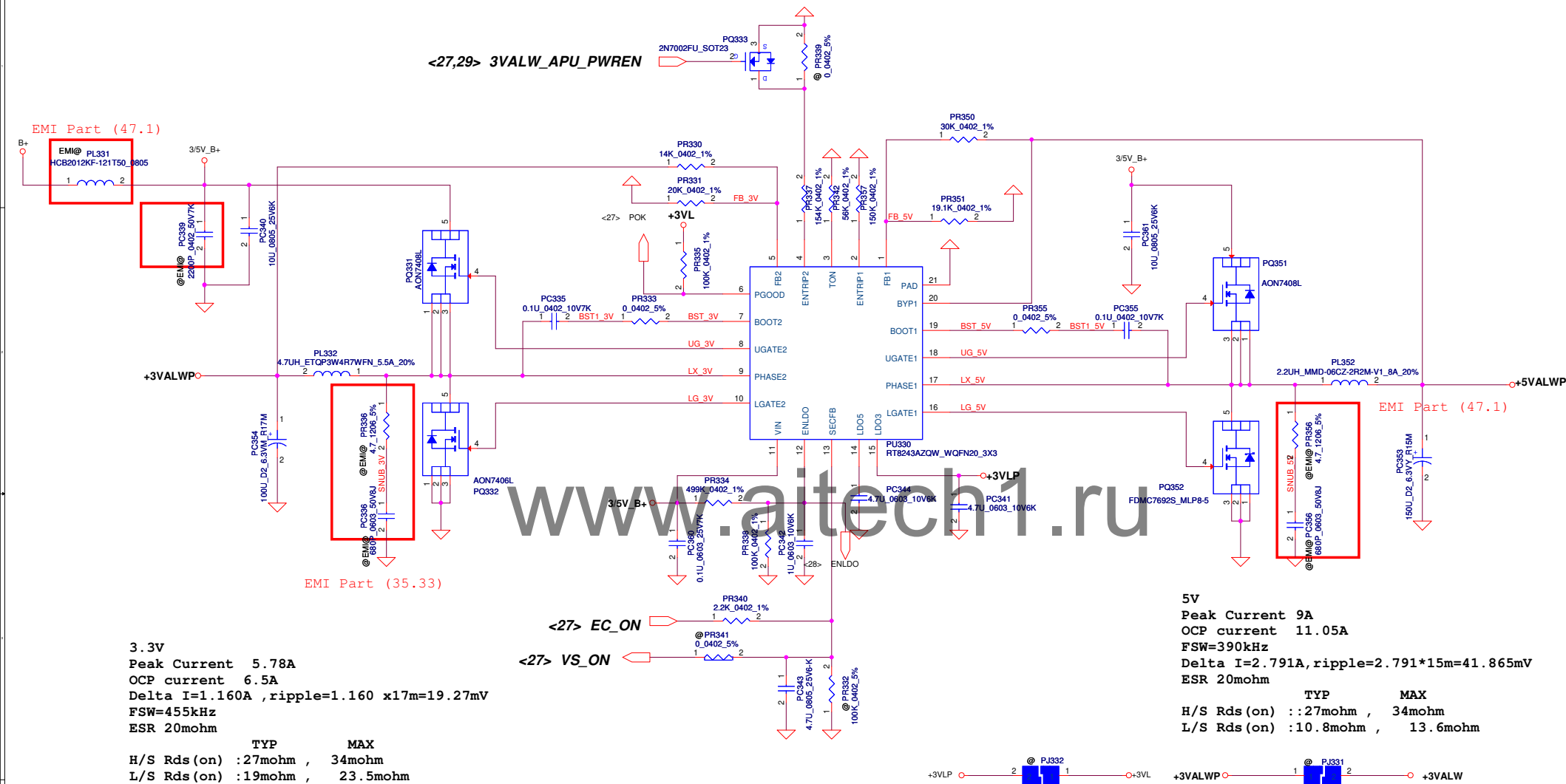
for reverse input protection

Charger controller (40.1), Support component (40.2)



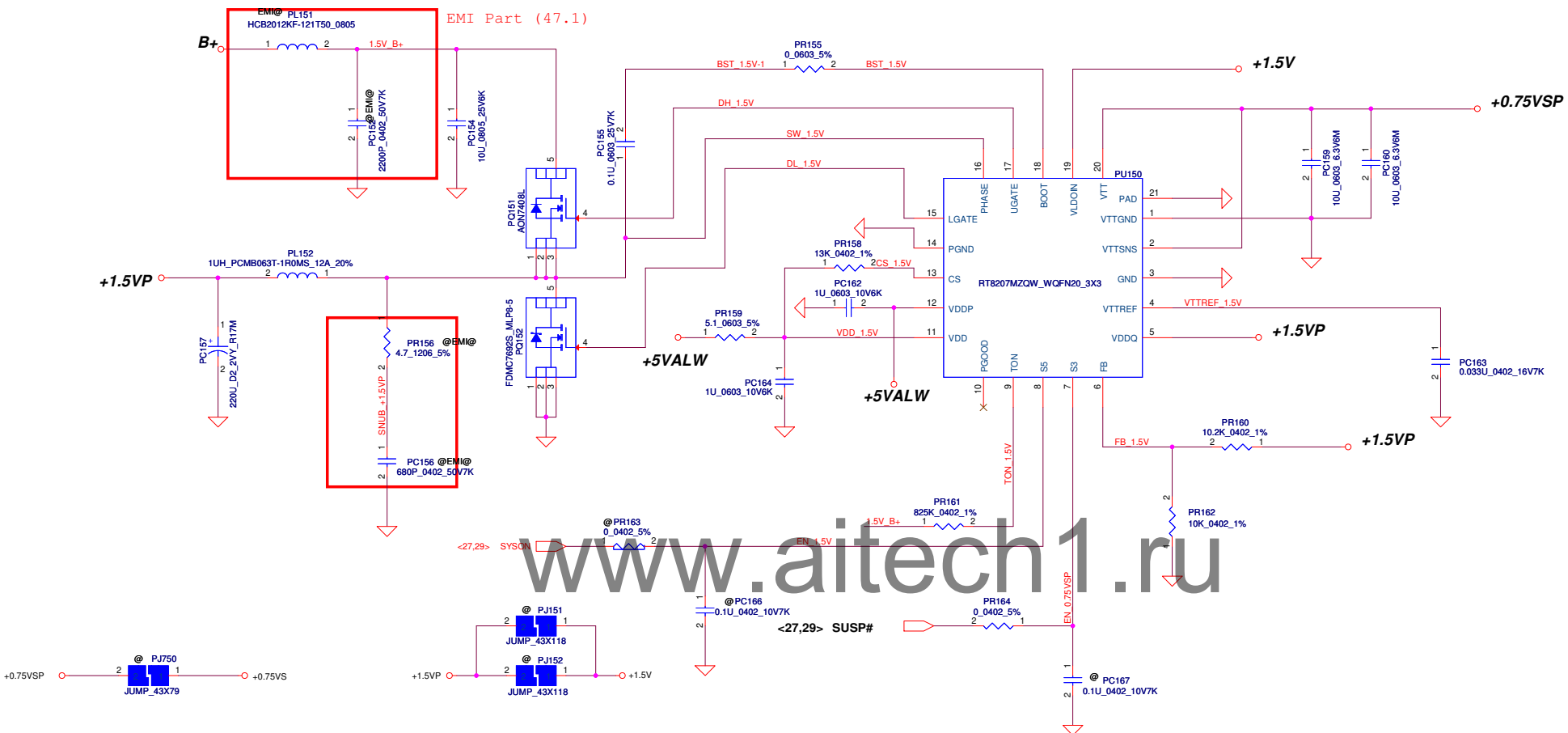
Security Classification		Compal Secret Data		Title	
Issued Date	2012/09/27	Deciphered Date	2015/09/27	Compal Electronics, Inc.	
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<27,29> 3VALW_APU_PWREN



Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Compal Electronics, Inc.	
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				Custom	LA-A551P
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DDR controller (35.3), Support component (35.4)



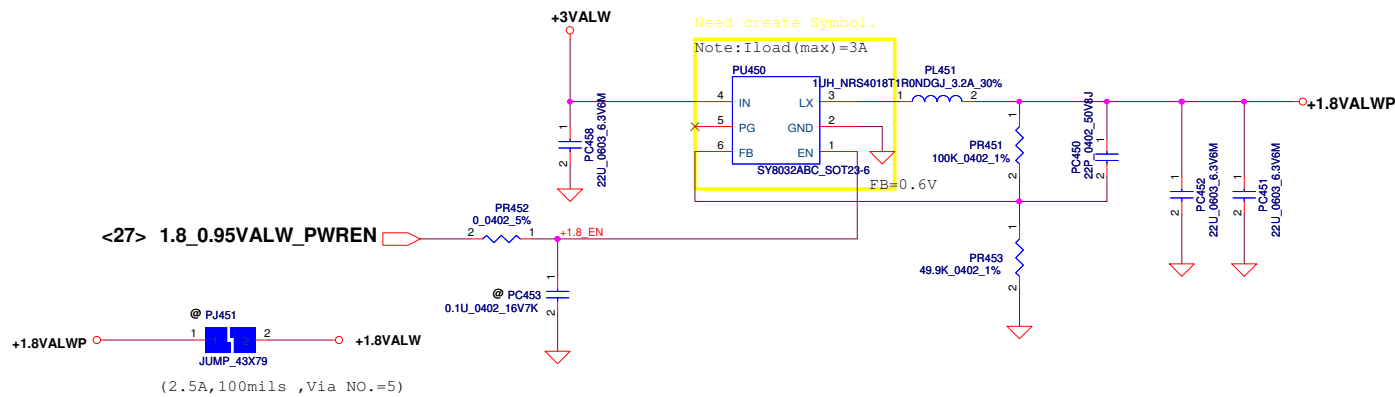
1.5V
Peak Current 8.1A
OCP current 9.63A
FSW=500kHz
DCR 8.3 ~ 10mohm
MAX
H/S Rds(on) : 27mohm , 34mohm
L/S Rds(on) : 10.8mohm , 13.6mohm

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

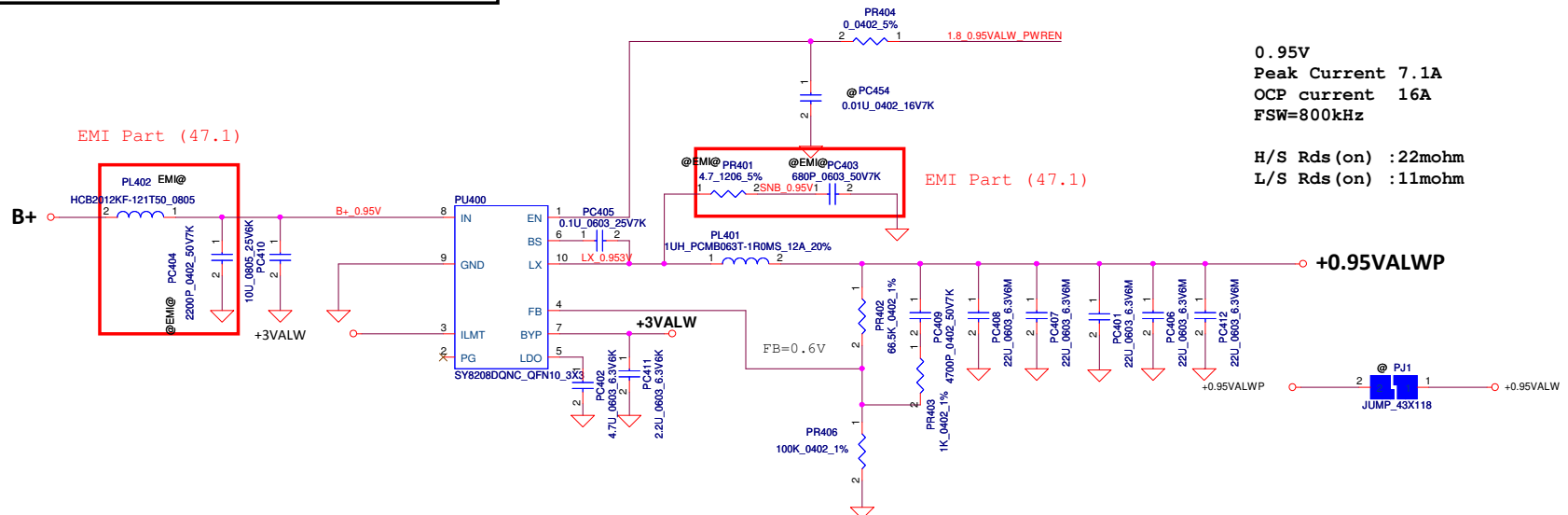
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title		
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				Size	Document Number	Rev
				Custm	LA-A551P	0.1
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1.8V controller (35.15), Support component (35.16)



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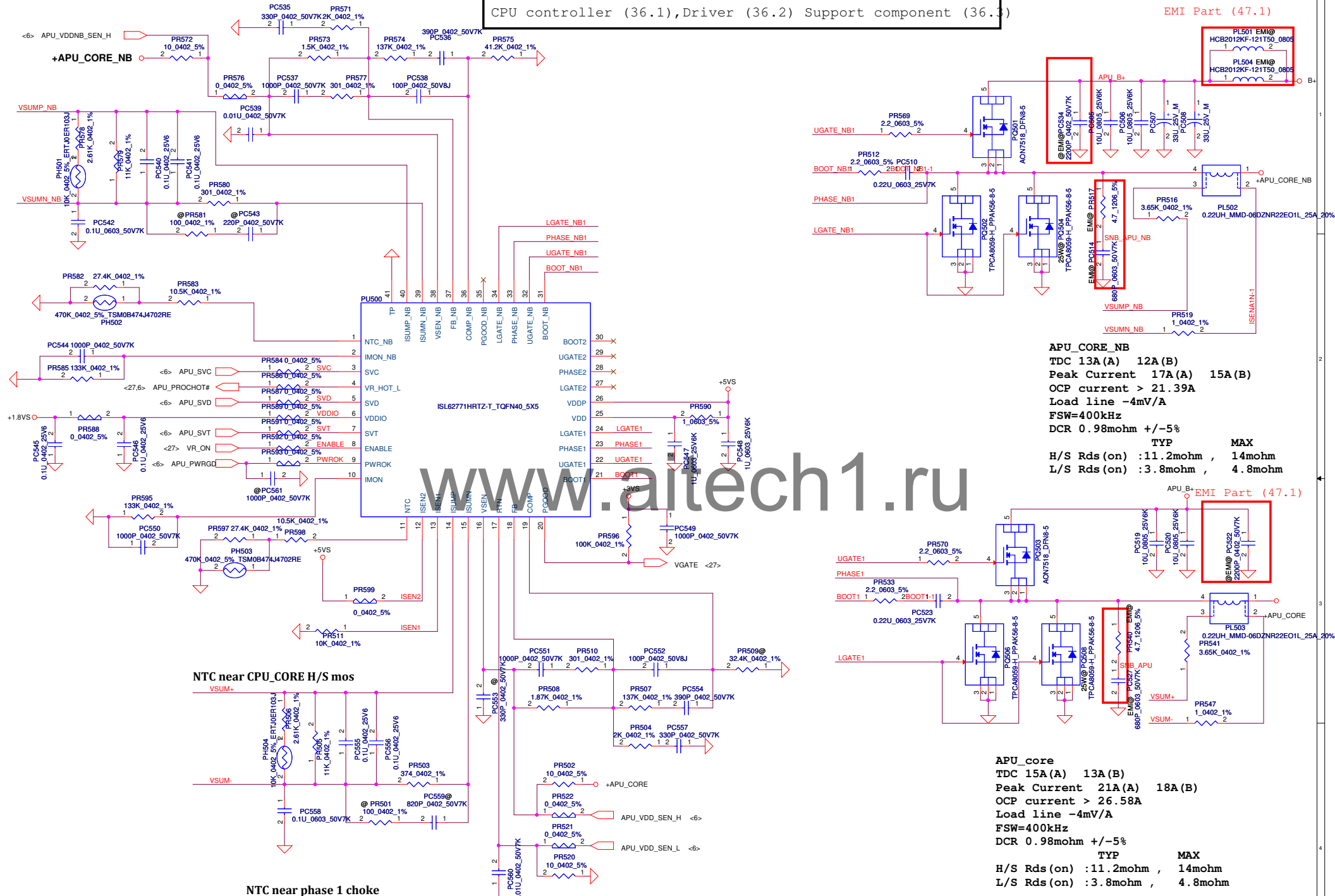
0.95V controller (35.27), Support component (35.28)



Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2012/09/27				Title			
				Deciphered Date				+1.8VALWP/+0.95VALWP			
								ZRM AE			
								Rev 0.1			
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								Sheet 35 of 40			

CPU controller (36.1),Driver (36.2) Support component (36.3)

EMI Part (47.1)



APU_CORE_NB
TDC 13A(A) 12A(B)
Peak Current 17A(A) 15A(B)
OCP current > 21.39A
Load line -4mV/A
FSW=400kHz
DCR 0.98mohm +/-5%

TYP MAX
H/S Rds(on) :11.2mohm , 14mohm
L/S Rds(on) :3.8mohm , 4.8mohm

APU_B+ EMI Part (47.1)

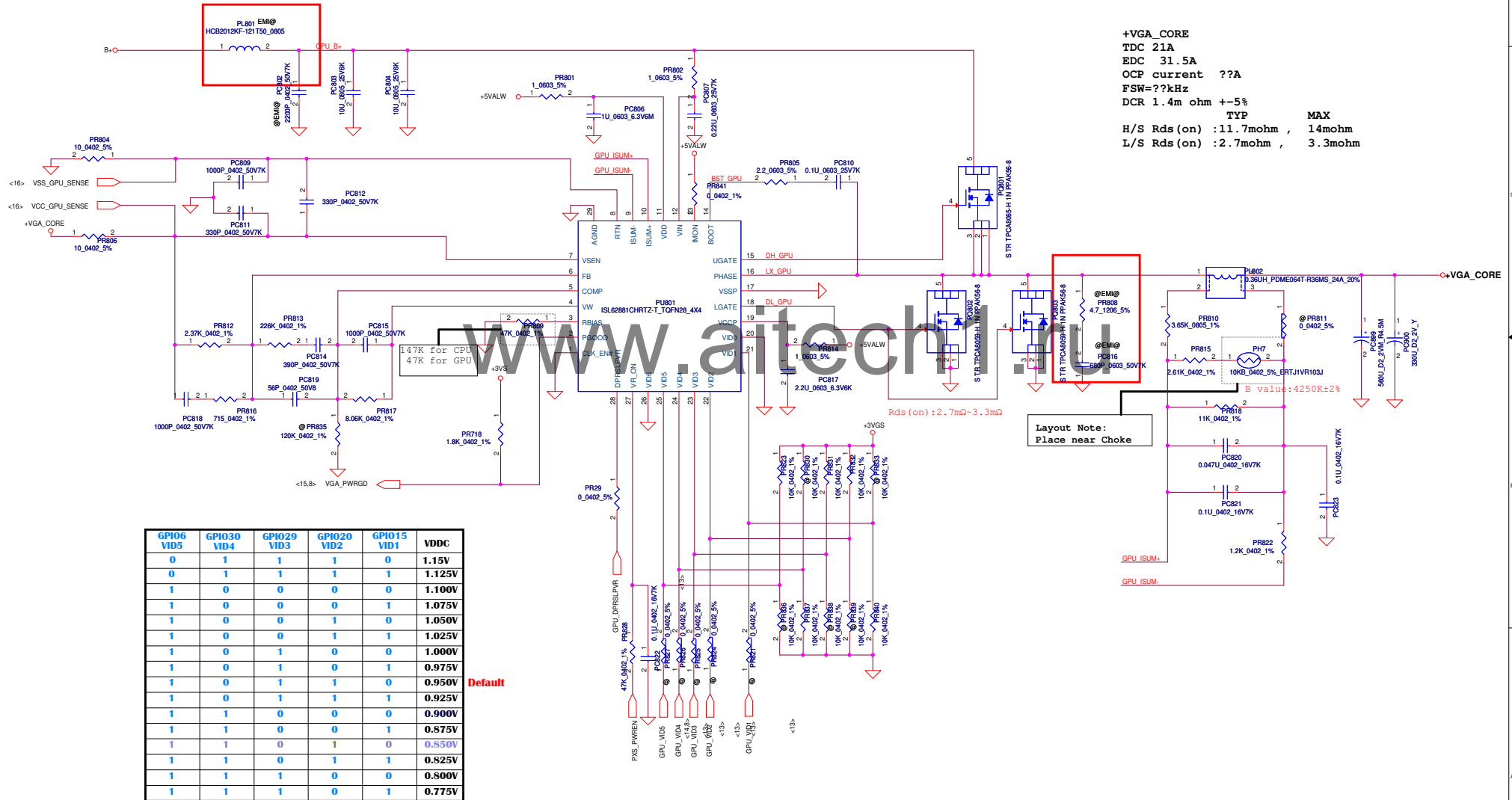
APU_core
TDC 15A(A) 13A(B)
Peak Current 21A(A) 18A(B)
OCP current > 26.58A
Load line -4mV/A
FSW=400kHz
DCR 0.98mohm +/-5%

TYP MAX
H/S Rds(on) :11.2mohm , 14mohm
L/S Rds(on) :3.8mohm , 4.8mohm

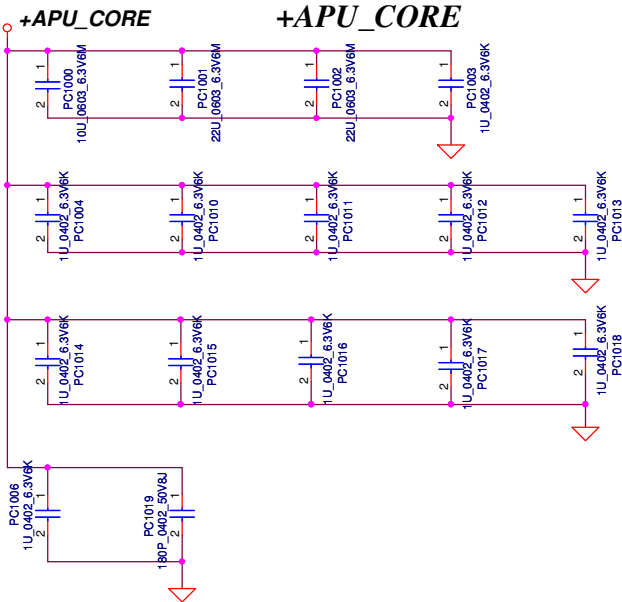
Security Classification		Compal Secret Data		Title	
Issued Date	2012/09/27	Deciphered Date		+CPU CORE/VDDNB	
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VGA controller (43.1),Driver (43.2) Support component (43.3)

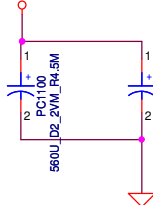
EMI Part (47.1)



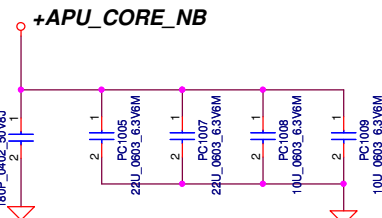
CPU_Core output CAP (Including MLCC) 36.4



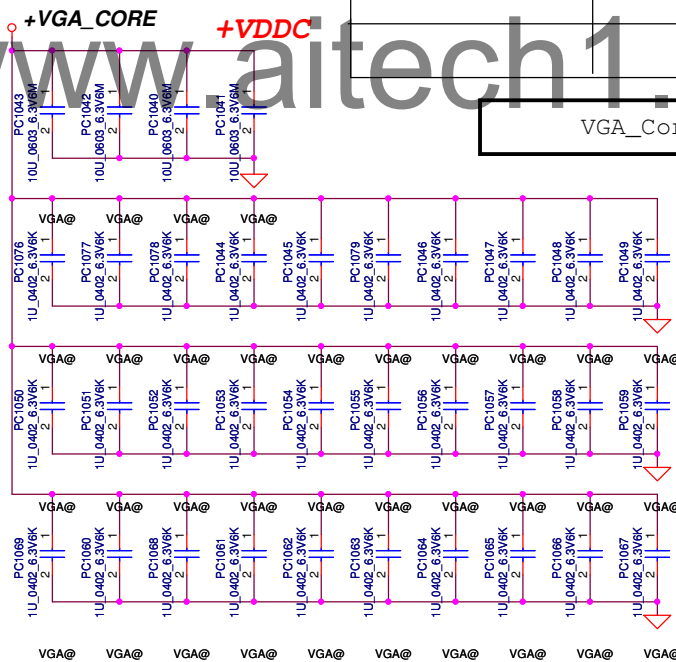
+APU_CORE



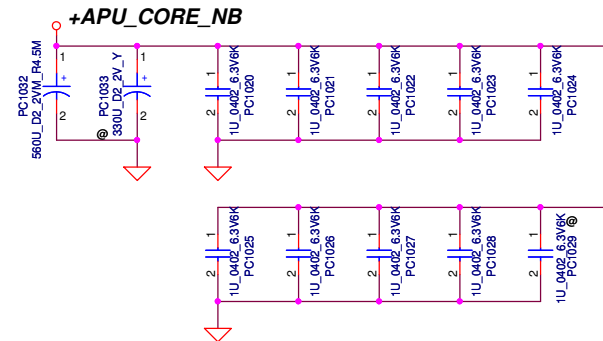
+APU_CORE_NB



+VGA_CORE



GFX output CAP (Including MLCC) 36.5



kABINI	560uF*4.5m	330uF	22uF (0603)	10uF (0603)	1u (0402)	180P (0402)
VDD	1	1	2	1	12	1
VDD_NB	1		2	2	9	1

VGA_Core output CAP (Including MLCC 43.9)

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for PWR

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								Size	Document Number	ZRM AE				Rev
								Custom					1.0	
								Date:		Tuesday, July 16, 2013		Sheet	39 of 40	

HW PIR (Product Improve Record)

ZEMAE LA-A551P SCHEMATIC CHANGE
LIST
REVISION CHANGE: 0.1 to 0.2

NO.	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	05/29	P24.	Delete RR2,RR3,RR7,RR6,RR12,RB7 for USB trace.	Part conut reduce
2.	05/29	P24.	Change CR13 to 0603.	HW4 Common design
3.	05/29	P24.	Delete SLP_CHG_CB0 & SLLP_CHG_CB1 from APU.	Reduce reserve
4.	05/29	P24,27,28.	EC_CHG_CB2(GPIO1A) move to GPIO12 、ADD NUM_LED#(JKB5.1 to JUB1.36)	Design change
5.	05/30	P08.	Add QC2 and connect HDMI_HDP_N to HDMI_HDP.	For HDMI utility
6.	05/30	P08.	Delete T24,T25,T27	For RTC issue
7.	05/30	P08.	Add RC3 15K pull down and reserve RC12,RC16,RC17 pull +3VALW_APU and RC5,RC11 pull gnd.	For RTC issue
8.	06/03	P24.	Change CR3&CR2 47u 0805 to CR6&CR10 and CR4&CR5 22u 0603	For hight limit
9.	06/03	P10.	Change CD43 from 47u 0805 to CD43&CD44 22u*2 0603	For hight limit
10.	06/03	P09.	Change CC14 from 47u 0805 to CC14&CC16 22u*2 0603	For hight limit
11.	06/07	P22.	Reserve varistor DL14 for LANGND to DGND	For ESD request
12.	06/07	P22.	Add diode DL5 for LANGND to DGND	For ESD request
13.	06/07	P26.	Remove RA18 and RA24	Remove reserve 0 ohm
14.	06/07	P25.	Add C18 0.1uF 0402 on +USB_VCCC close to JSB5	For EMI request
15.	06/10	P20.	Change C17 form 1500P to 0.015uF	For LCD sequence
16.	06/10	P25.	Remove 0ohm for 14 and 15 and add LR10 and LR9	For part count reduce
17.	06/11	P26.	Change LA7 and LA6 form 0402 to 0603 size	For EMI request
18.	06/11	P25.	Swap LR7/LR8 pin1&4 and pin3&2	For layout smooth
19.	06/11	P24.	Add test point for S&C IC T10&T11&T24	For NPI debug
20.	06/13	P28.	Change H4&H5 form H_3P3 to H_3P2	For ME limite
21.	06/14	P21.	Colay RY4,RY5,RY6,RY7,RY8,RY9,RY10,RY11 with HDMI check	For EMI request

ZEMAE LA-A551P SCHEMATIC CHANGE
LIST
REVISION CHANGE: 0.2 to 1.0

NO.	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	07/05	A11	Change R2,R130,RC116,RC117,RC119,RC120,R106,RA22,RA25,RA1,RA21,LA8 to shortpad	MP Part reduce
2.	07/05	P28	Delete SW5	Remove debug part
3.	07/05	P29	Reserve QC1B	Remove non-used part
4.	07/05	P06	Add APU_CRT_R/G/B pull 75ohm to GND	For disable CRT
5.	07/05	P08	Change CC31 form 10P to 8PF	XTRAL PPM fine tune
6.	07/08	P28	Change H20 screw hole to 2.7mm from 2.8mm	ME change
7.	07/08	P08	Add RC11 15K pull GND	AMD request
8.	07/08	P26	Change LA8 shortpad form 0402 to 0603	EMI request
9.	07/11	P28	Change C24 100pF cap to D32 100p varistor	ESD request
10.	07/15	P24	Update PCB footprint	DFB request

Title		
HW PIR		
Size	Document Number	Rev
B	LA-A551P	1.0
Date:	Tuesday, July 16, 2013	Sheet 40 of 40